4.5.3 – 168 PIN UNBUFFERED DRAM DIMM FAMILY

CAPACITY—256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, & 64M WORDS OF 64, 72, OR 80 BITS

DATA CONFIGURATIONS—Four DATA Word configurations are defined:
—64 BIT without PARITY
—72 BIT for PARITY CODES
—72 BIT & 80 BIT for ECC CODES

CONFIGURATION—13 Different Configurations are defined using various combinationa of X1, X4, X8, X16 and X18 memories.

LOGIC FEATURES—The modules contain “SERIAL PRESENCE DETECT” features using EEPROM stored information that profided a variety of encoded information regarding the module such as storage capacity, configuration, data word configuration, refresh mode, and speed of the module.
—Check Bit locations are pre–assigned

PACKAGE—168 PIN JEDEC DIMM MEMORY MODULE

PIN ASSIGNMENTS—Figs. 4.5.3–A, & 4.5.3–B

SPD TABLES—Figs. 4.5.3–C

KEYING METHODOLOGY—Fig. 4.5.3–D

CONFIGURATION BLOCK DIAGRAM—Figs. 4.5.3–E through 4.5.3–U

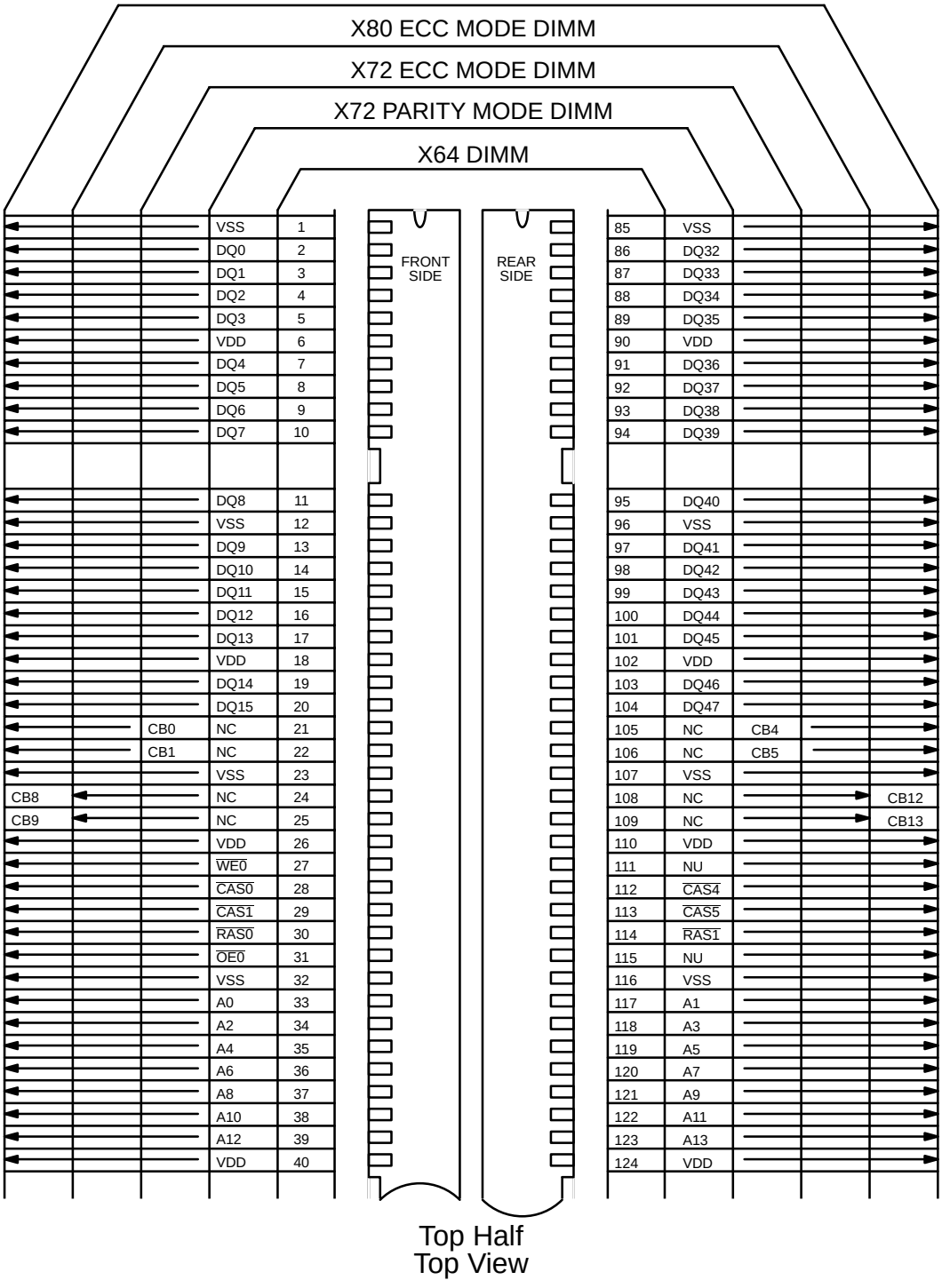


FIGURE 4.5.3–A
168 Pin, 64, 72, or 80 BIT DIMM PINOUT, TOP HALF

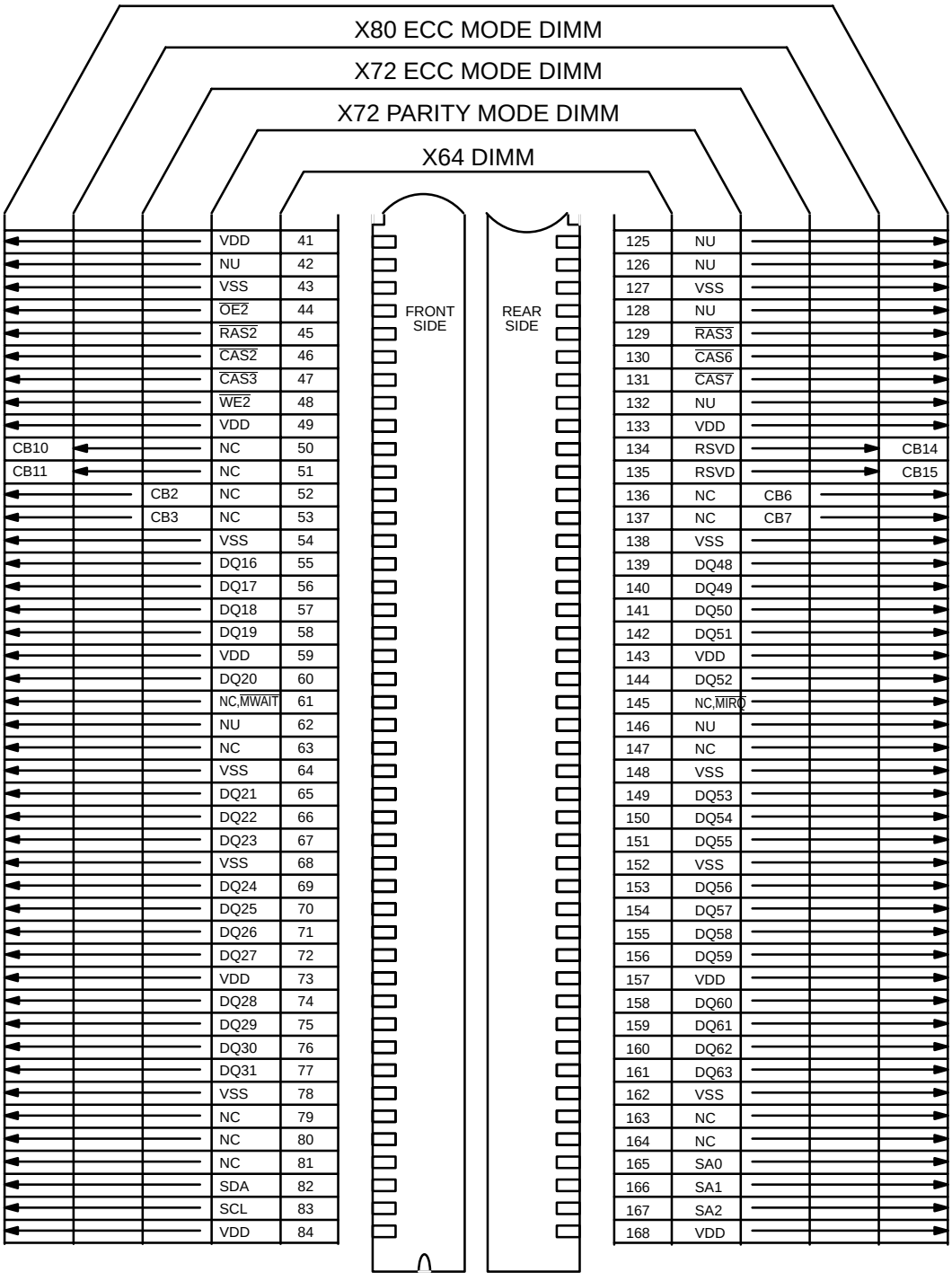
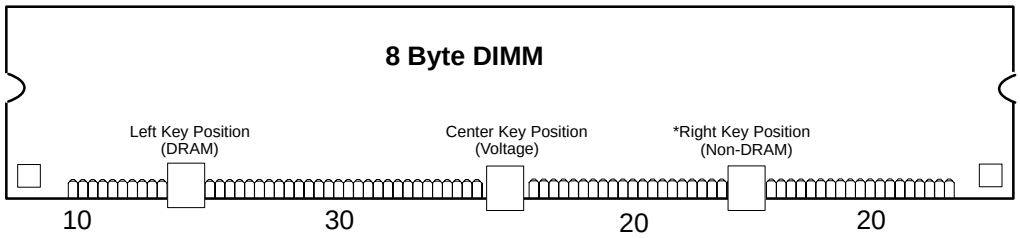
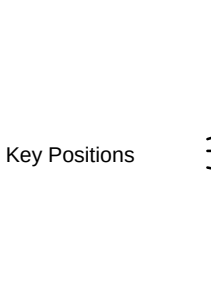


FIGURE 4.5.3–B
168 Pin, 64, 72, or 80 BIT DIMM PINOUT, BOTTOM HALF

Buffered	Unbufffered
All signals except RAS and Data are buffered	No buffers, all DRAM signals are connected directly to DIMM tab pins
11 Pins are used for DIMM attributes (PDE, PD1-8, ID0-1)	5 pins are used for DIMM attributes (SDA, SCL, SA0-2)
CAS Pin assignment sequence optimized for buffer placement 0, 1 2, 3 4, 5 6, 7	CAS Pin signals are re-assigned for optimal DRAM placement 0, 4 1, 5 2, 6 3, 7
ECC DIMMs use subset of CAS signals for word selection (CAS0/1 and CAS4/5)	All DIMM types use byte selection (CAS0-7)
Address 0 to the DRAMs is sourced from separate pins (A0, B0) for 4 byte interleave	Single address pin (A0)
Data pin assignment uses both X64/X72 and X80 numbering schemes	Data pin assignment is changed to single x80 numbering scheme with x64 and x72 as subsets
Non-Parity is subset of Parity with inter-mixed Parity bits unconnected (PQ8, 17, 26, 35, 44, 53, 62, 71)	All DIMM types use the same sequential 64 data pins (DQ0-63). Eight center pins (CB0-7) are used as Parity/Check Bits for x72 Parity/ECC DIMMs. An additional 8 center pins (CB8-15) are used for the x80 ECC DIMMs.
32 Power/Gnd Pins V_{CC} - 16 V_{SS} - 16	35 Power/Gnd Pins V_{CC} - 17 (1 additional pin) V_{SS} - 18 (2 additional pins)
Unused Pins - 18	Unused Pins - 14
Left Key Definition SDRAM STD DRAM RFU	Left Key Definition modified RFU Buffered Assembly (DRAM/SDRAM) Unbuffered Assembly (DRAM/SDRAM)

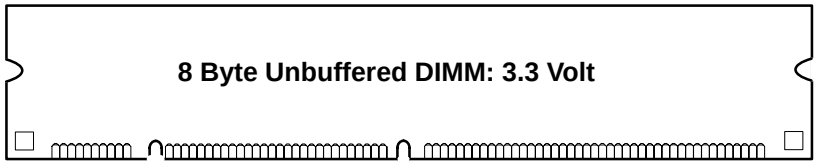
FIGURE 4.5.3–C
Comparison of 168 Pin Buffered & Unbuffered DRAM & SDRAM DIMM





Left Key	Center Key	*Right Key
RFU	5V	No Key
BUFFERED ASSEMBLY	3.3V	No Key
UNBUFFERED ASSEMBLY	X.XV	No Key

* For DRAM/SDRAM assemblies, this area is poplulated with pads.



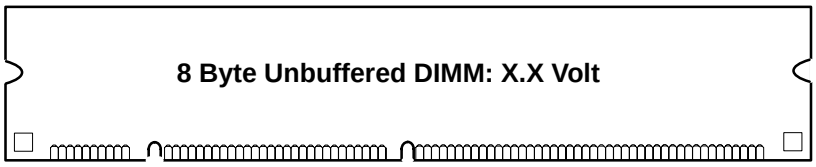


FIGURE 4.5.3–D
168 Pin DRAM DIMM Keying Methodology

Pin #	DRAM DIMM	SDRAM DIMM
28	$\overline{CAS0}$	DQMB0
29	$\overline{CAS1}$	DQMB1
30	$\overline{RAS0}$	S0
31	$\overline{OE}0$	NU
39	A12	BA1
42	NU	CK0
44	$\overline{OE}2$	NU
45	$\overline{RAS}2$	$\overline{S}2$
46	$\overline{CAS}2$	DQMB2
47	$\overline{CAS}3$	DQMB3
48	$\overline{WE}2$	NU
62	NU	V_{REF} (IF APPLICABLE)
63	NC	CKE1
79	NU	CK2
111	NU	$\overline{CAS}$
112	$\overline{CAS}4$	DQMB4
113	$\overline{CAS}5$	DQMB5
114	$\overline{RAS}1$	$\overline{S}1$
115	NU	$\overline{RAS}$
122	A11	BA0
123	A13	A11
125	NU	CK1
126	NU	A12
128	NU	CKE0
129	$\overline{RAS}3$	$\overline{S}3$
130	$\overline{CAS}6$	DQMB6
131	$\overline{CAS}7$	DQMB7
132	NU	A13
146	NU	V_{REF} (IF APPLICABLE)
163	NC	CK3

Notes:
1. A10 on DRAM DIMM is also AP on SDRAM DIMM
2. A11 on DRAM DIMM is also BS0 on SDRAM DIMM
3. A12 on DRAM DIMM is also BS1 on SDRAM DIMM (for 4 Bank SDRAMs)

FIGURE 4.5.3–E
Pinout Comparison, 168 Pin DRAM & SDRAM DIMM

8 Byte Presence Detect Information

- Serial PD Interface Protocol: IIC (Synchronous 2-Wire Bus)
- The following information is to be written into EEPROM device during module production:

a. Module Configurations, Addressing: (Bytes 3-7)

Module Configuration	DRAM Organization	Option 1		Option 2		Option 3	
		$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.	$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.	$\overline{RAS}$ Addr.	$\overline{CAS}$ Addr.
256K x 64/72/80	256K x 16	9	9				
512K x 64/72/80	256K x 16	9	9				
512K x 64/72/80	512K x 8	10	9				
512K x 64	512K x 32	10	9	12	7		
1M x 64/72/80	512K x 8	10	9				
1M x 64/72/80	1M x 4/16/18	10	10	12	8		
1M x 64	512K x 32	10	9	12	7		
2M x 64/72/80	1M x 4/16/18	10	10	12	8		
2M x 64/72/80	2M x 8	11	10	12	9		
2M x 64	2M x 32	12	9	13	8		
4M x 64/72/80	2M x 8	11	10	12	9		
4M x 64/72/80	4M x 4/16/18	11	11	12	10	*13	9
4M x 64	2M x 32	12	9	13	8		
8M x 64/72/80	4M x 4/16/18	11	11	12	10	*13	9
8M x 64/72/80	8M x 8	12	11	13	10		
8M x 64	8M x 32	TBD	TBD				
16M x 64/72/80	8M x 8	12	11	13	10		
16M x 64/72/80	16M x 4/16/18	12	12	13	11	*14	10
16M x 64	8M x 32	TBD	TBD				
32M x 64/72/80	16M x 4/16/18	12	12	13	11	*14	10
32M x 64/72/80	32M x 8	TBD	TBD				
32M x 64	32M x 32	TBD	TBD				
64M x 64/72/80	32M x 8	TBD	TBD				
64M x 64/72/80	64M x 4	TBD	TBD				
64M x 64	32M x 32	TBD	TBD				

(Note: All options possible with DRAM standards are shown)
* This addressing option applies to x16 and x18 DRAM configuration

b. Allowable configurations: (Byte 11)
  - x64 (Non-parity, Byte controls)
  - x72 (Parity, Byte controls)
  - x72 (ECC-optimized, Byte controls)
  - x80 (ECC-optimized, Byte controls)

c. Functional Attributes:
  - Power Supply Voltage/Interface levels (Byte 8)
  - $\overline{RAS}$ access (Byte 9)
  - $\overline{CAS}$ access (Byte 10)
  - Refresh rate/type (Byte 12)

Figure 4.5.3–F
168 Pin UNBUFFERED DRAM DIMM SPD ASSIGNMENTS

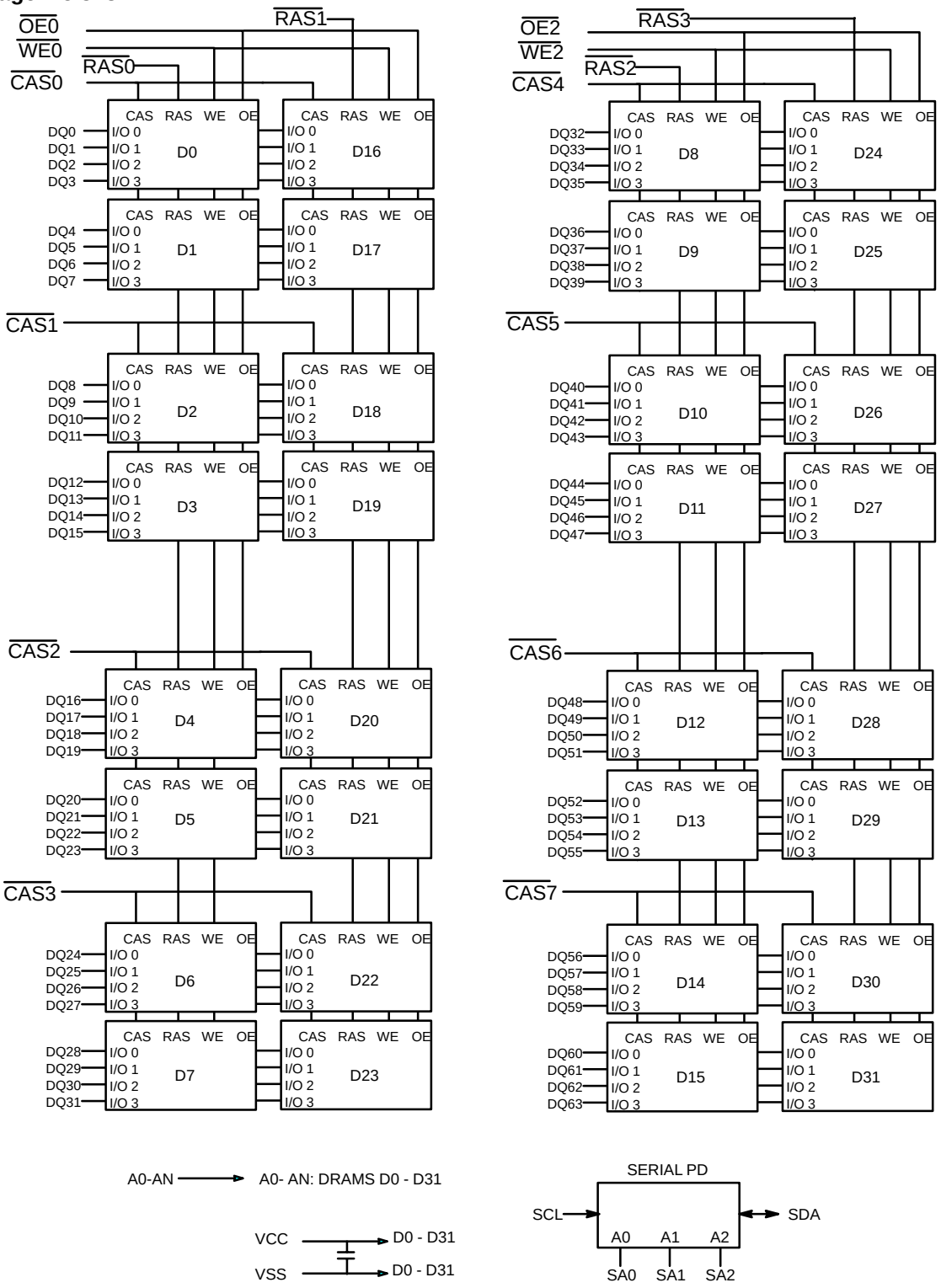


Figure 4.5.3–G
168 Pin, X64 DRAM DIMM, 2 Banks with X4 DRAMs

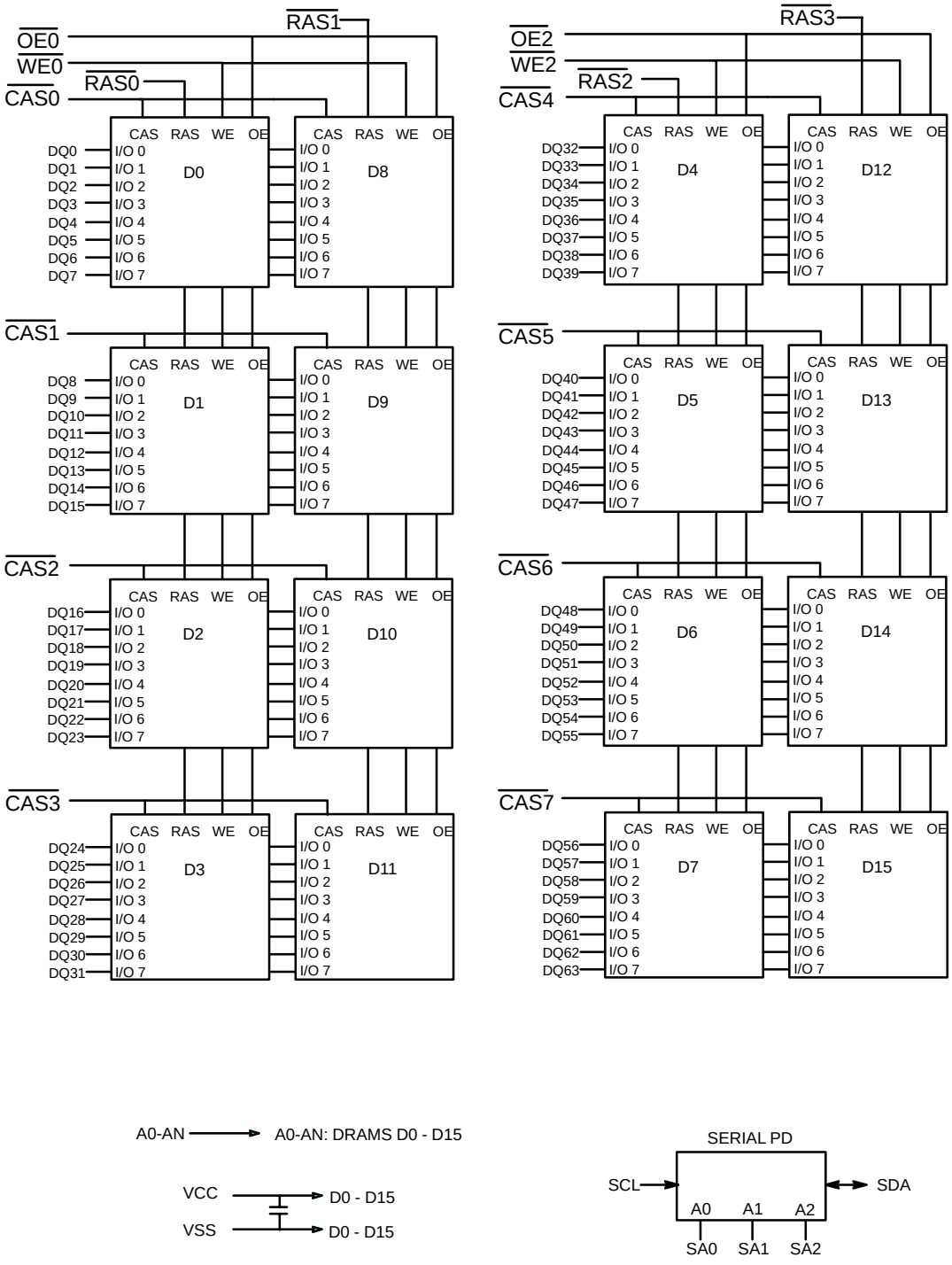


Figure 4.5.3–H
168 Pin, X64 DRAM DIMM, 2 Banks with X8 DRAMs

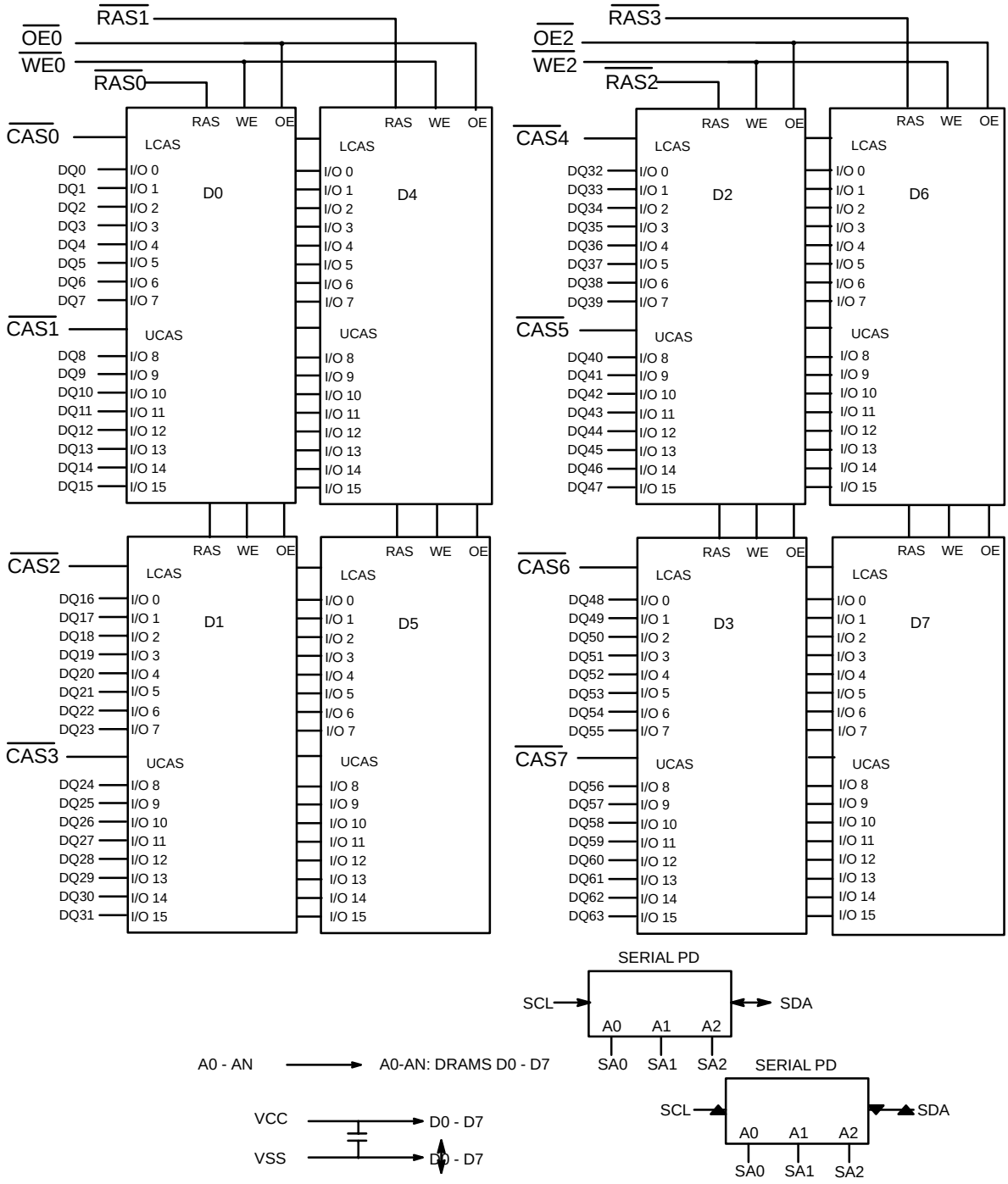


Figure 4.5.3–I
168 Pin, X64 DRAM DIMM, 2 Banks with X16 DRAMs

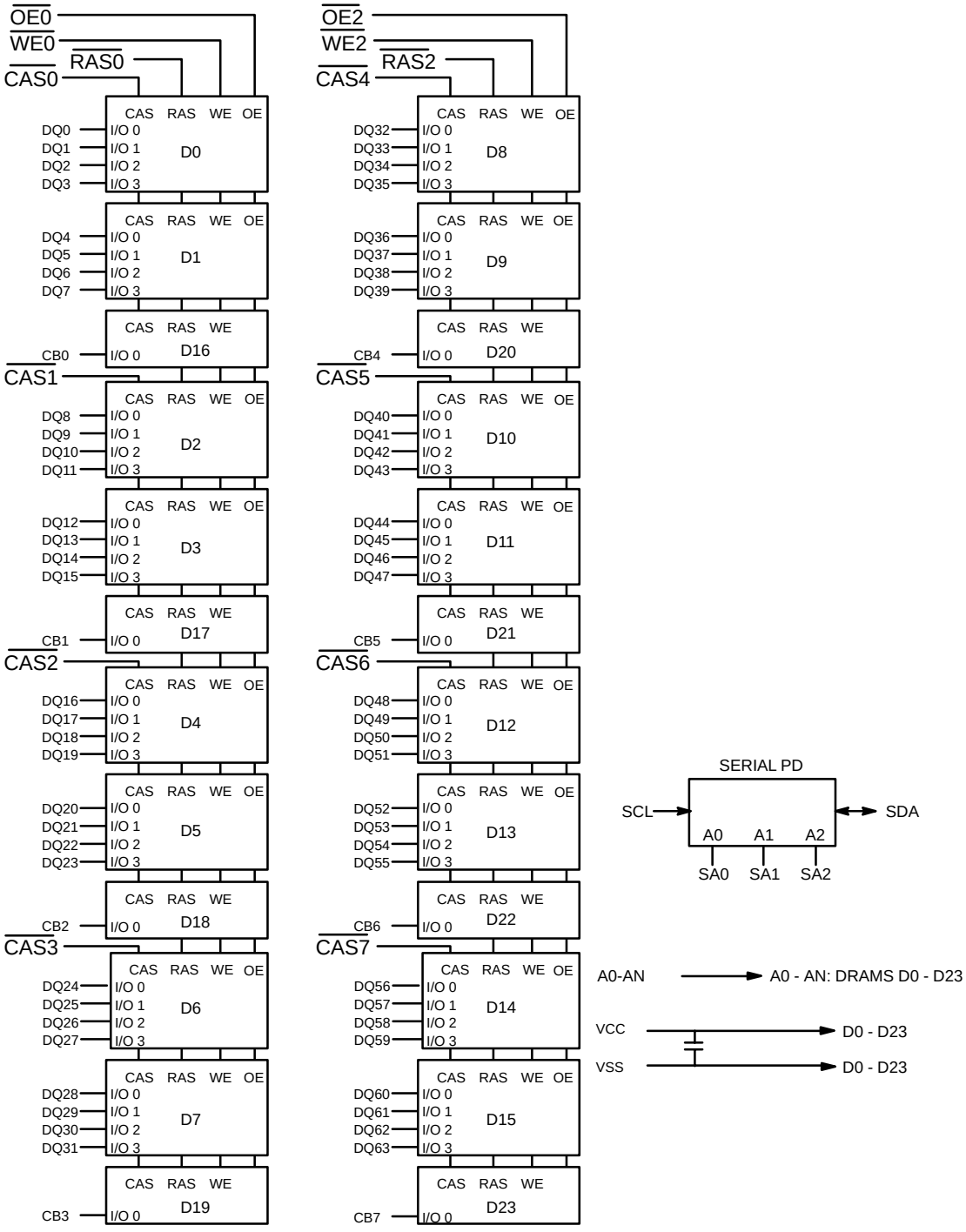


Figure 4.5.3–J
168 Pin, X64 DRAM DIMM, 2 Banks with X4/X1 DRAMs

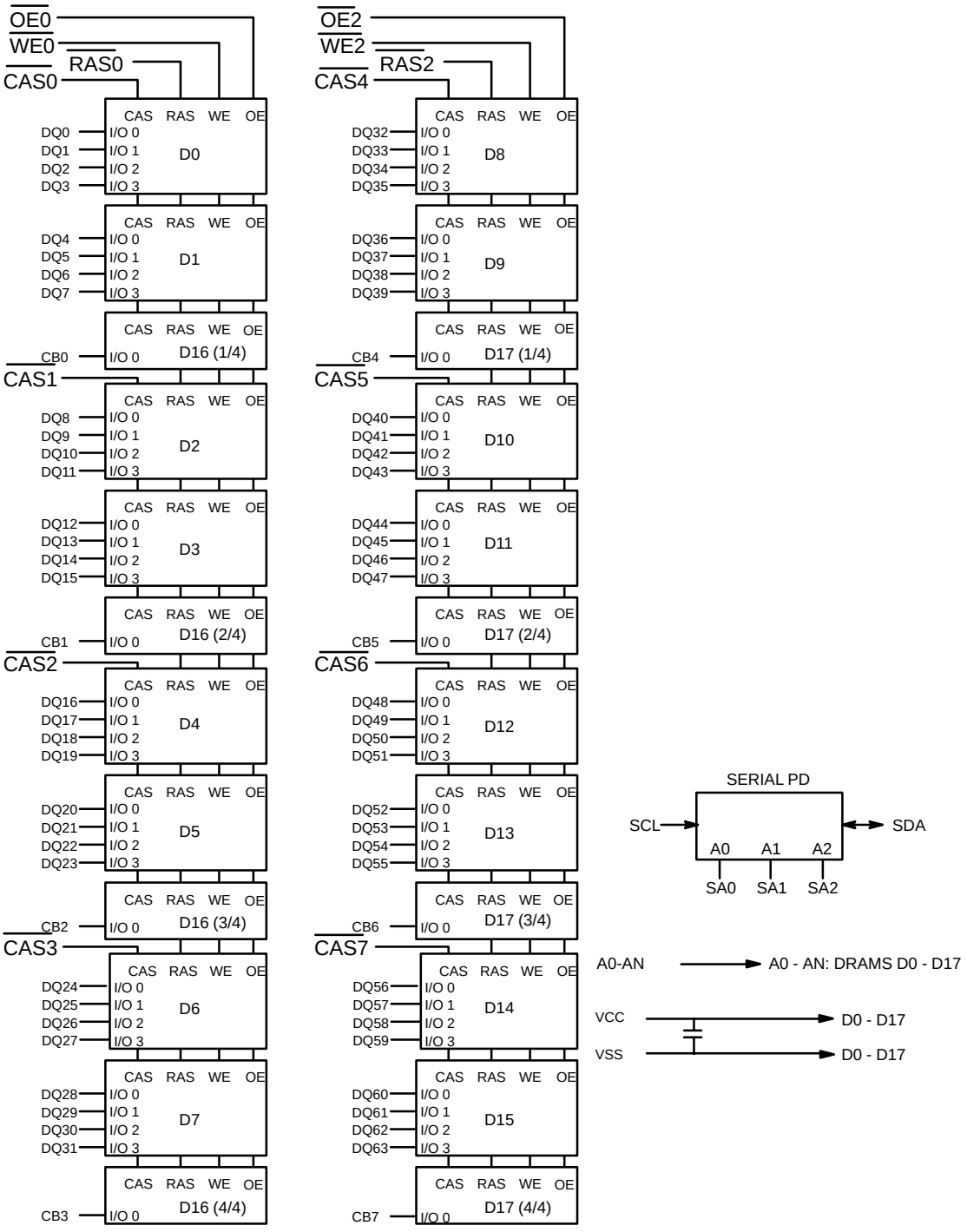


Figure 4.5.3–K
168 Pin, X72 Parity DRAM DIMM, 2 Banks with X4 & X4 W/4 CAS DRAMs

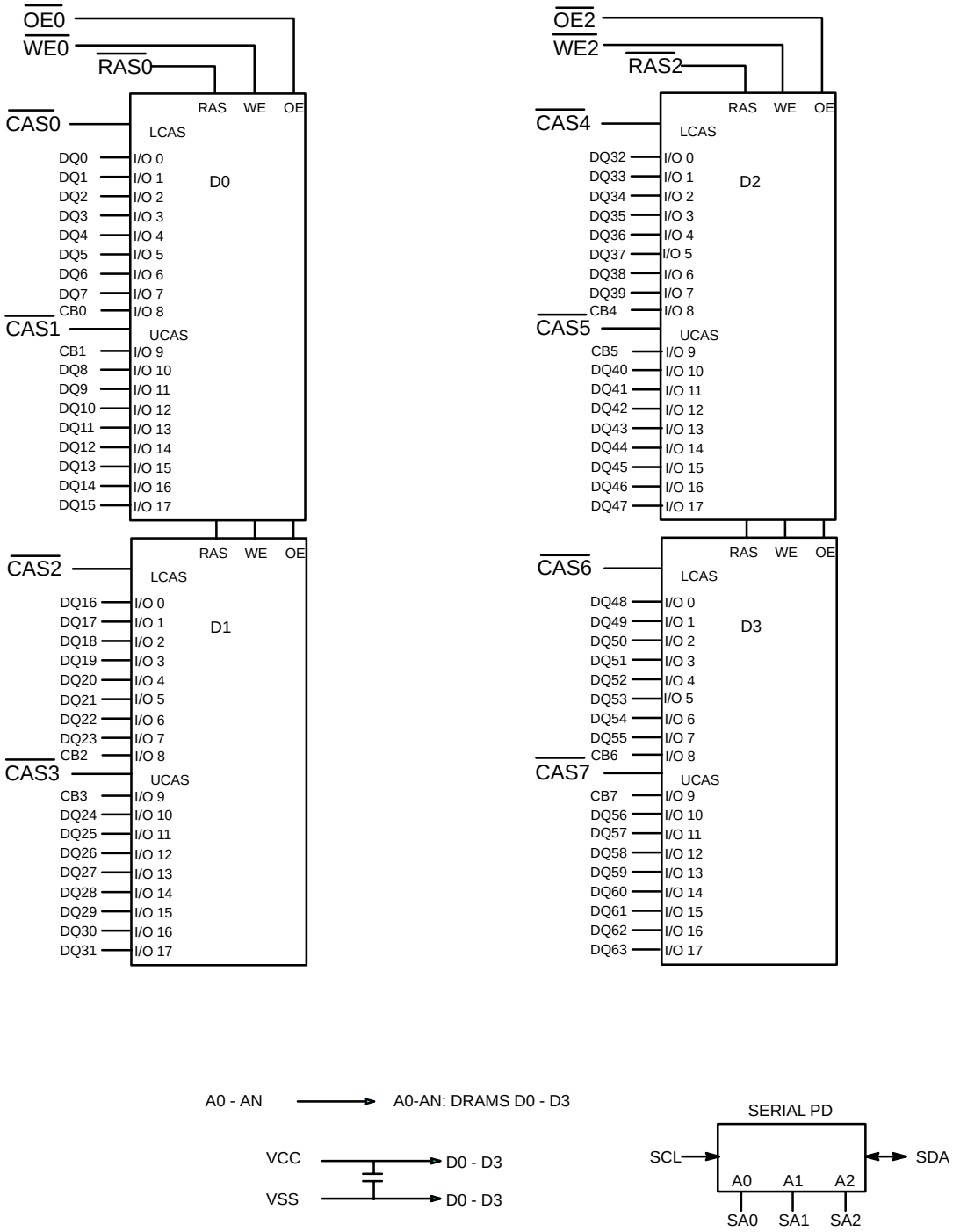


Figure 4.5.3–L
168 Pin, X72 Parity DRAM DIMM, 2 Banks with X16 DRAMs

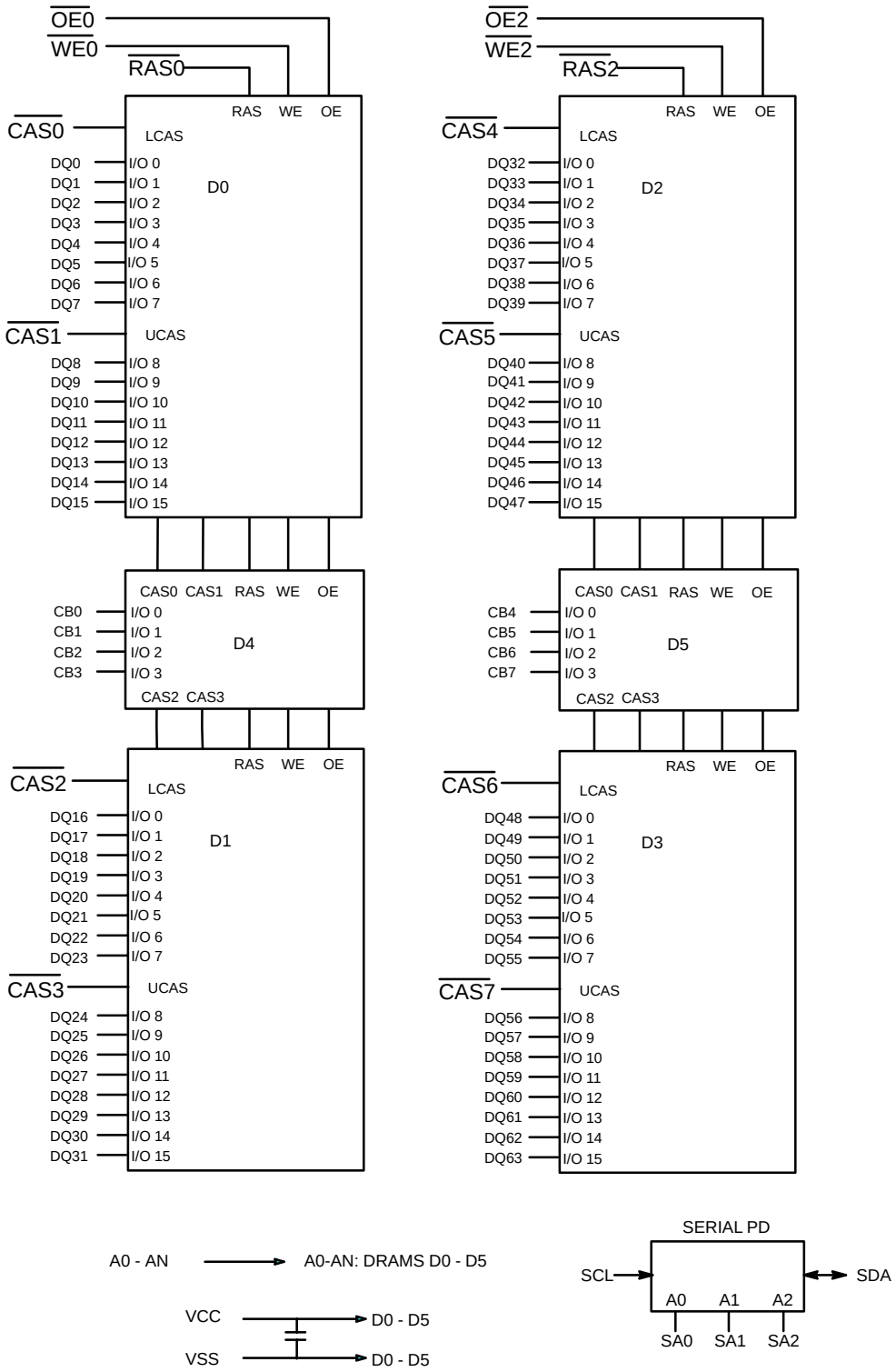


Figure 4.5.3–M
168 Pin, X72 Parity DRAM DIMM, 2 Banks with X16 & X4 W/4 CAS DRAMs

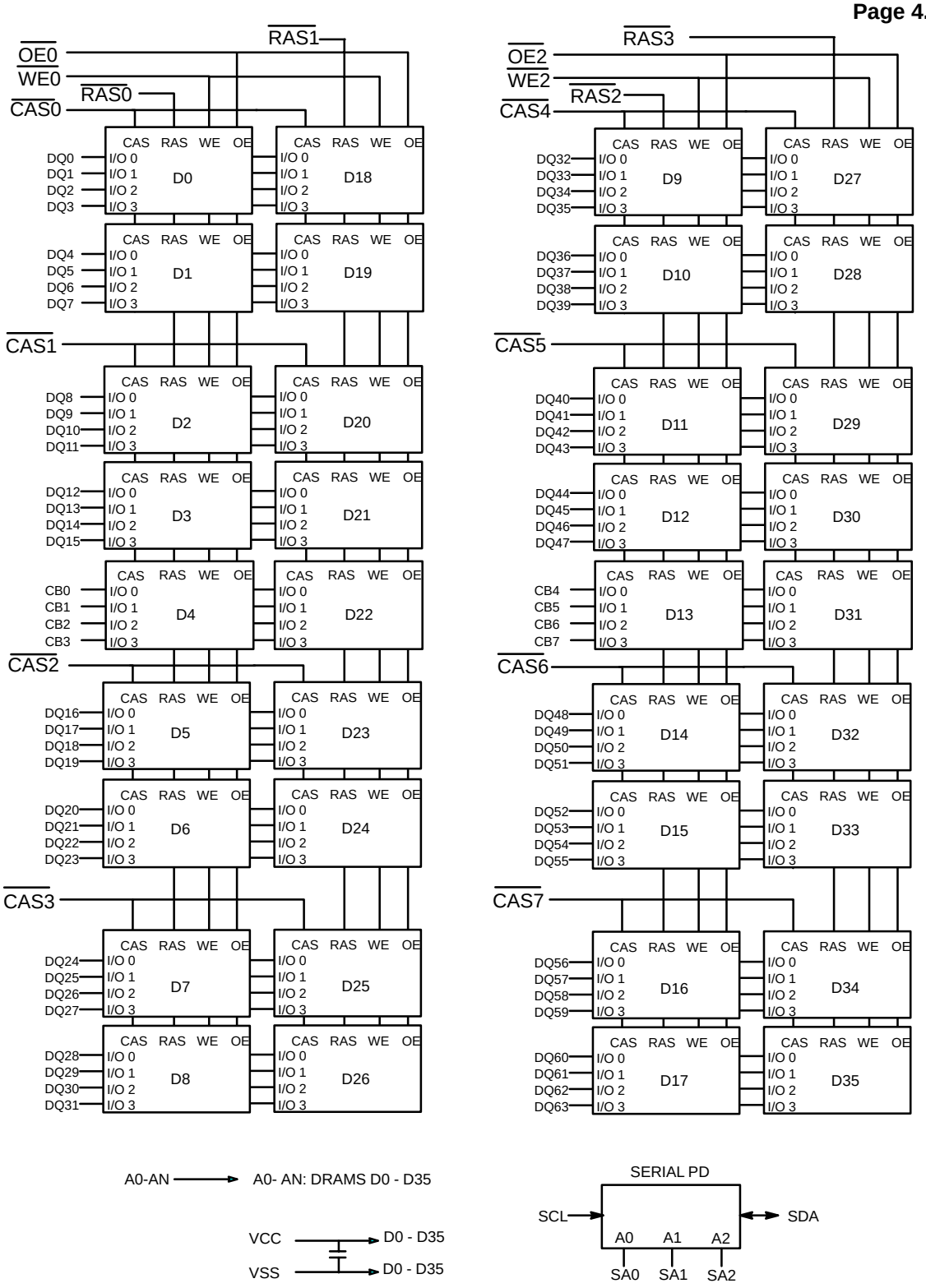


Figure 4.5.3–N
168 Pin, X72 ECC DRAM DIMM, 2 Banks with X4 DRAMs

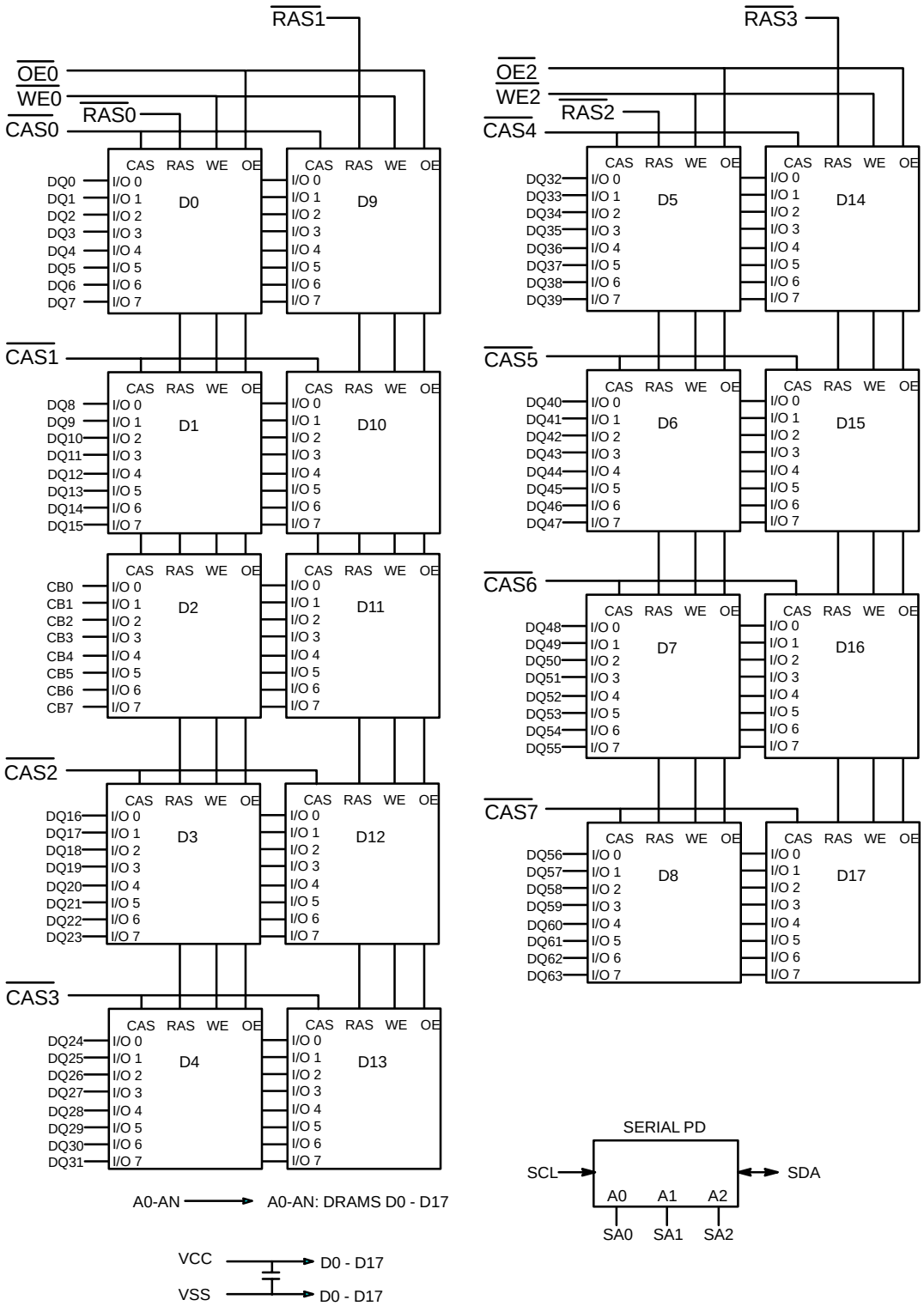


Figure 4.5.3–O
168 Pin, X72 ECC DRAM DIMM, 2 Banks with X8 DRAMs

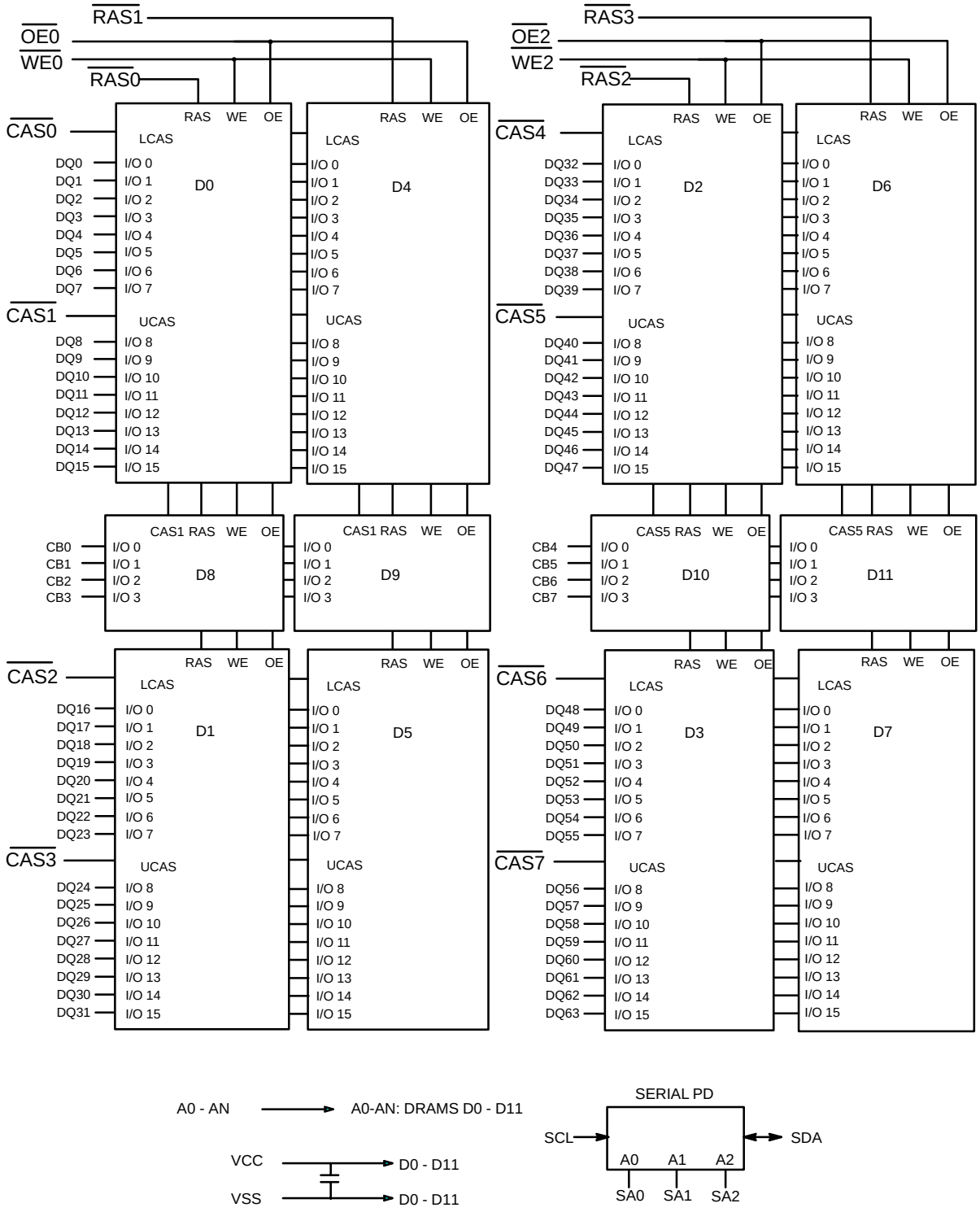


Figure 4.5.3–P
168 Pin, X72 ECC DRAM DIMM, 2 Banks with X16 & X4 DRAMs

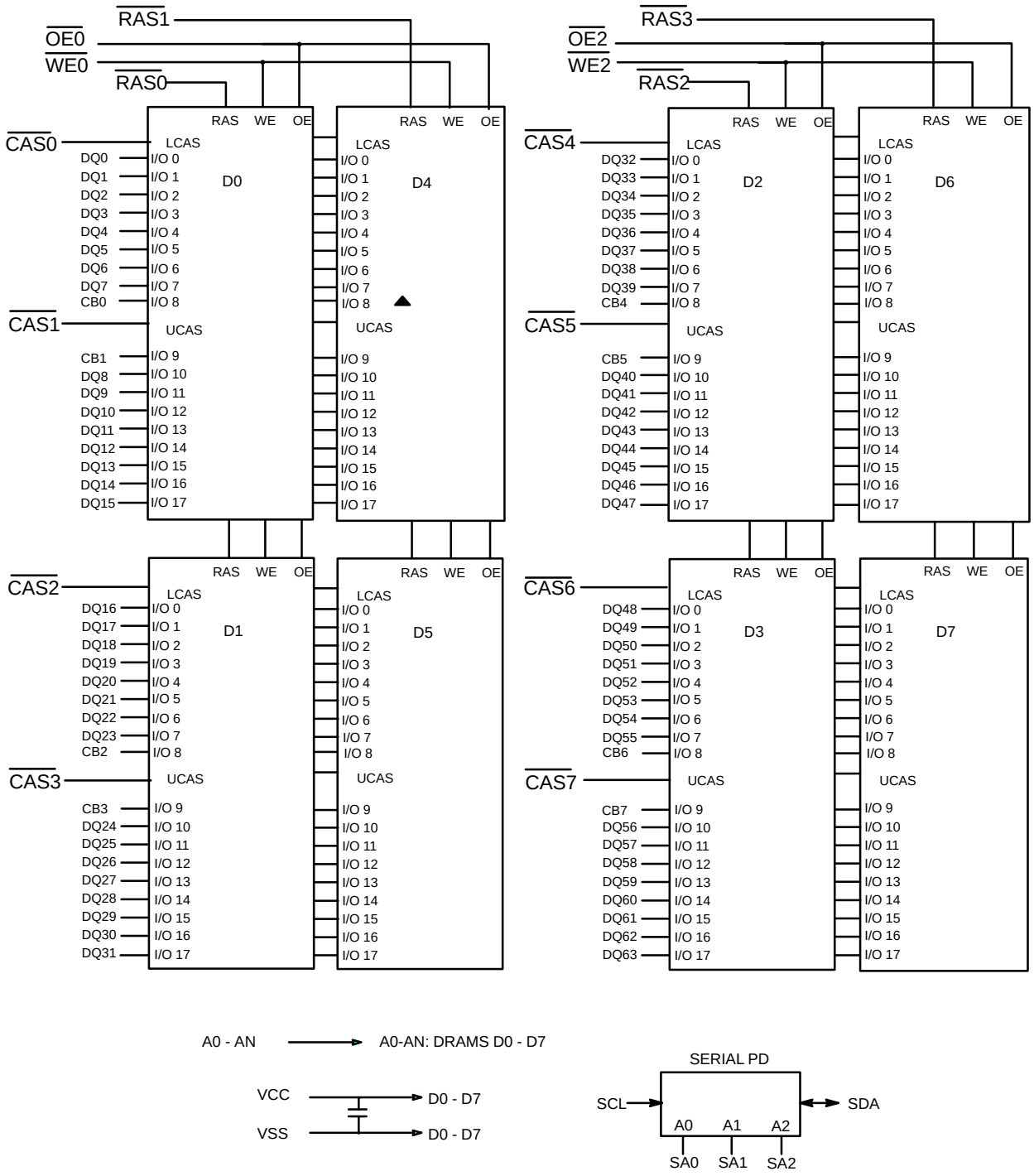


Figure 4.5.3–Q
168 Pin, X72 ECC DRAM DIMM, 2 Banks with X18 DRAMs

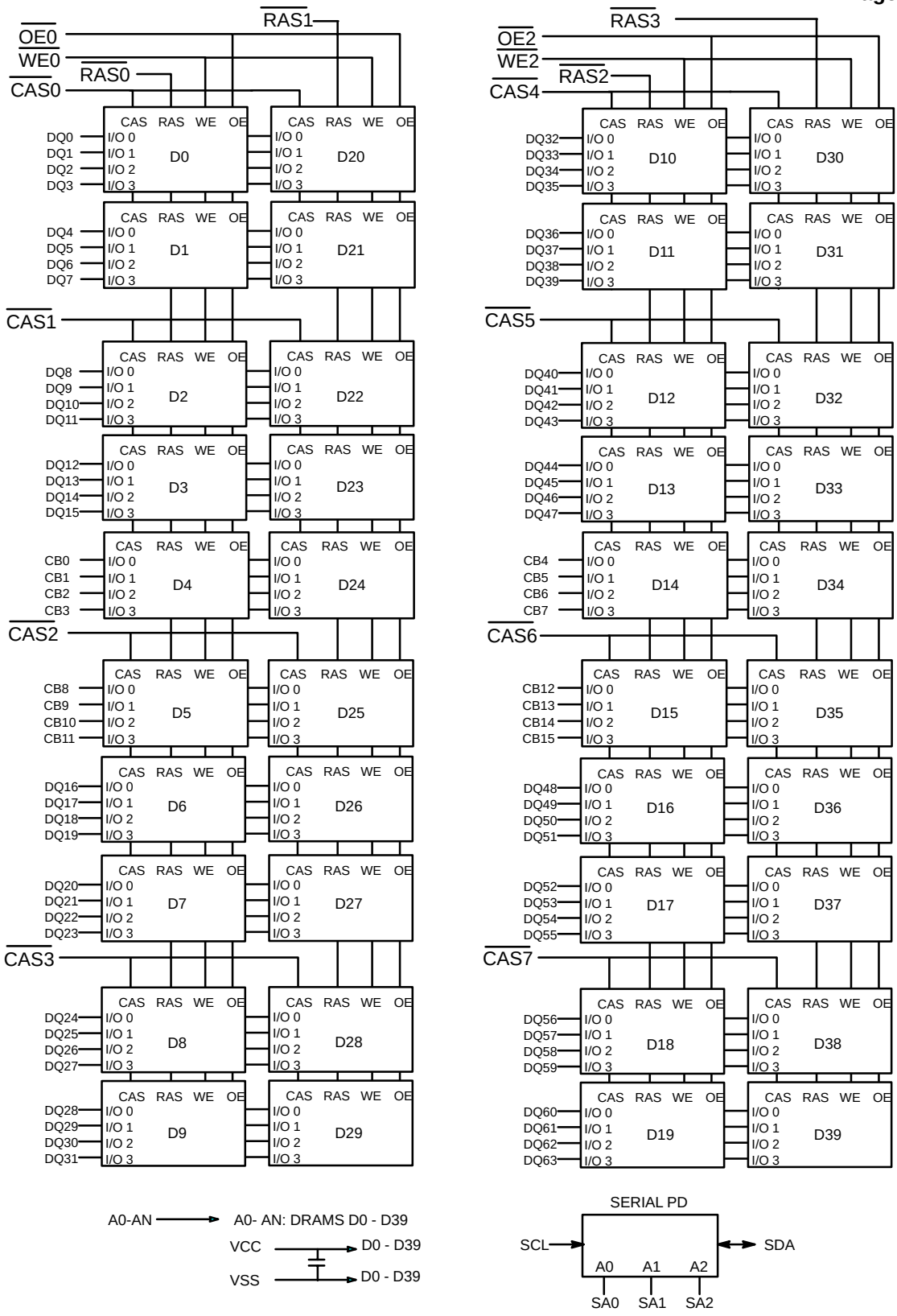


Figure 4.5.3–R
168 Pin, X80 DRAM DIMM, 2 Banks with X4 DRAMs

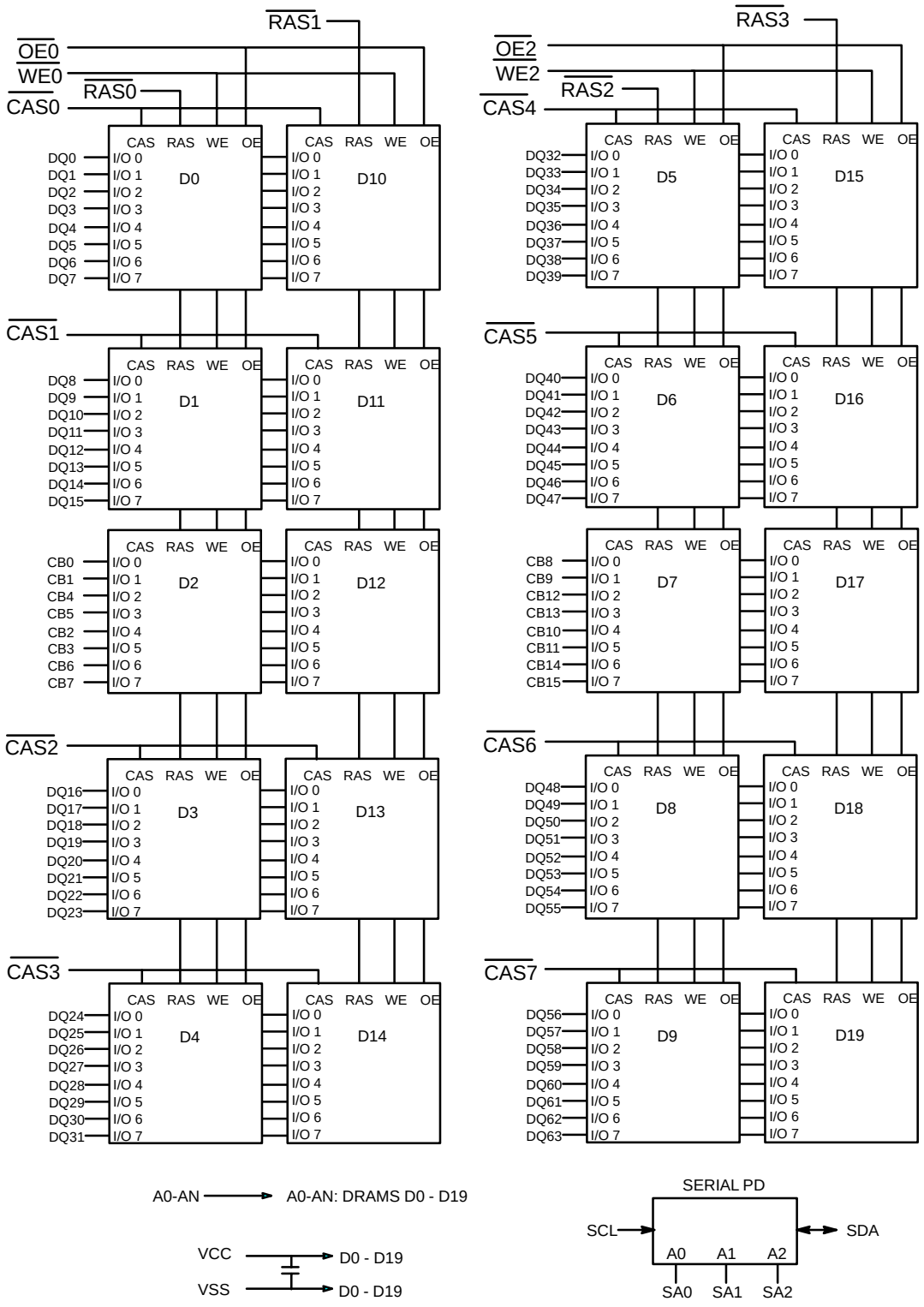


Figure 4.5.3–S
168 Pin, X80 ECC DRAM DIMM, 2 Banks with X8 DRAMs

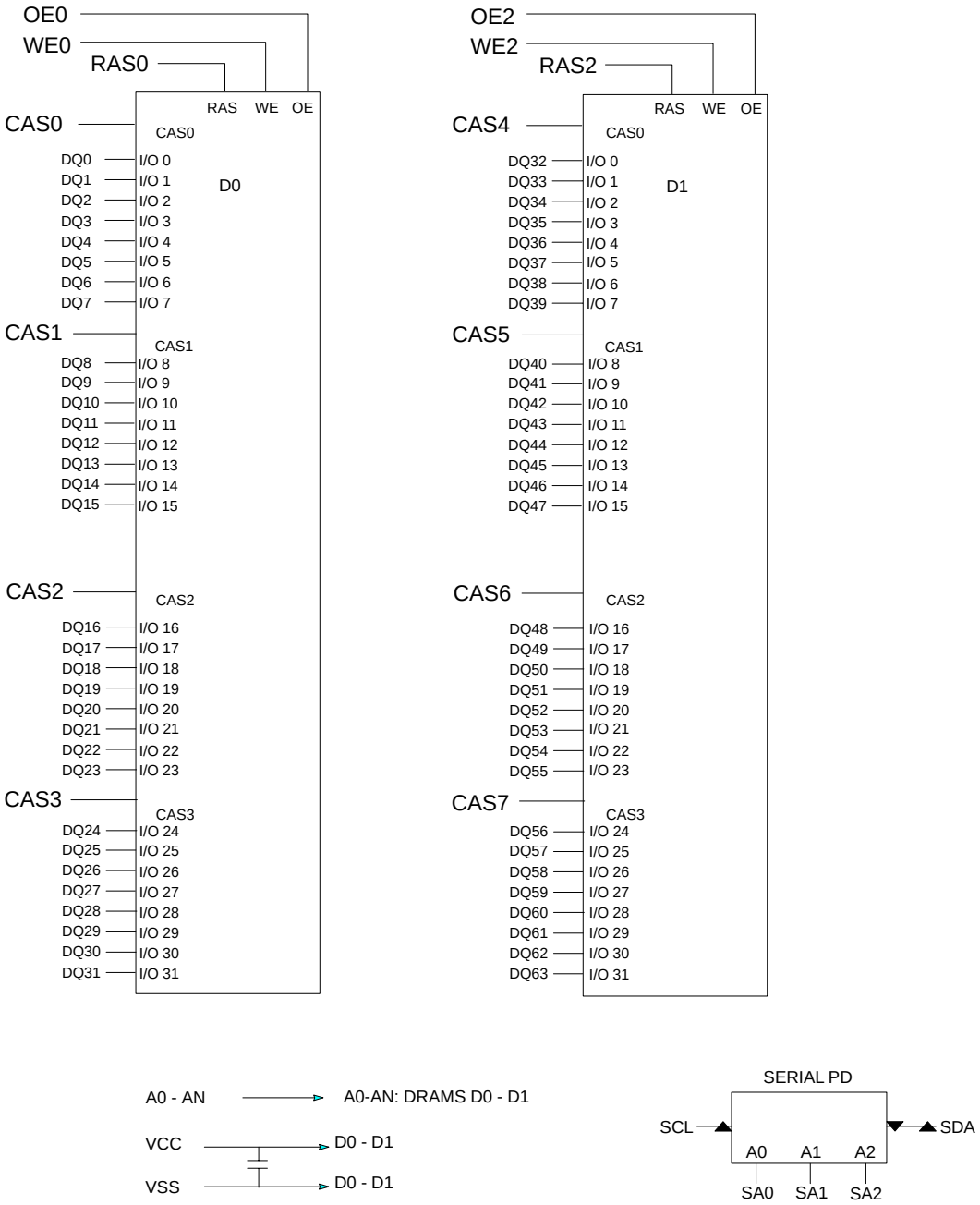


Figure 4.5.3–T
168 Pin X64 DRAM DIMM, 1 BANK, X32 DRAMs

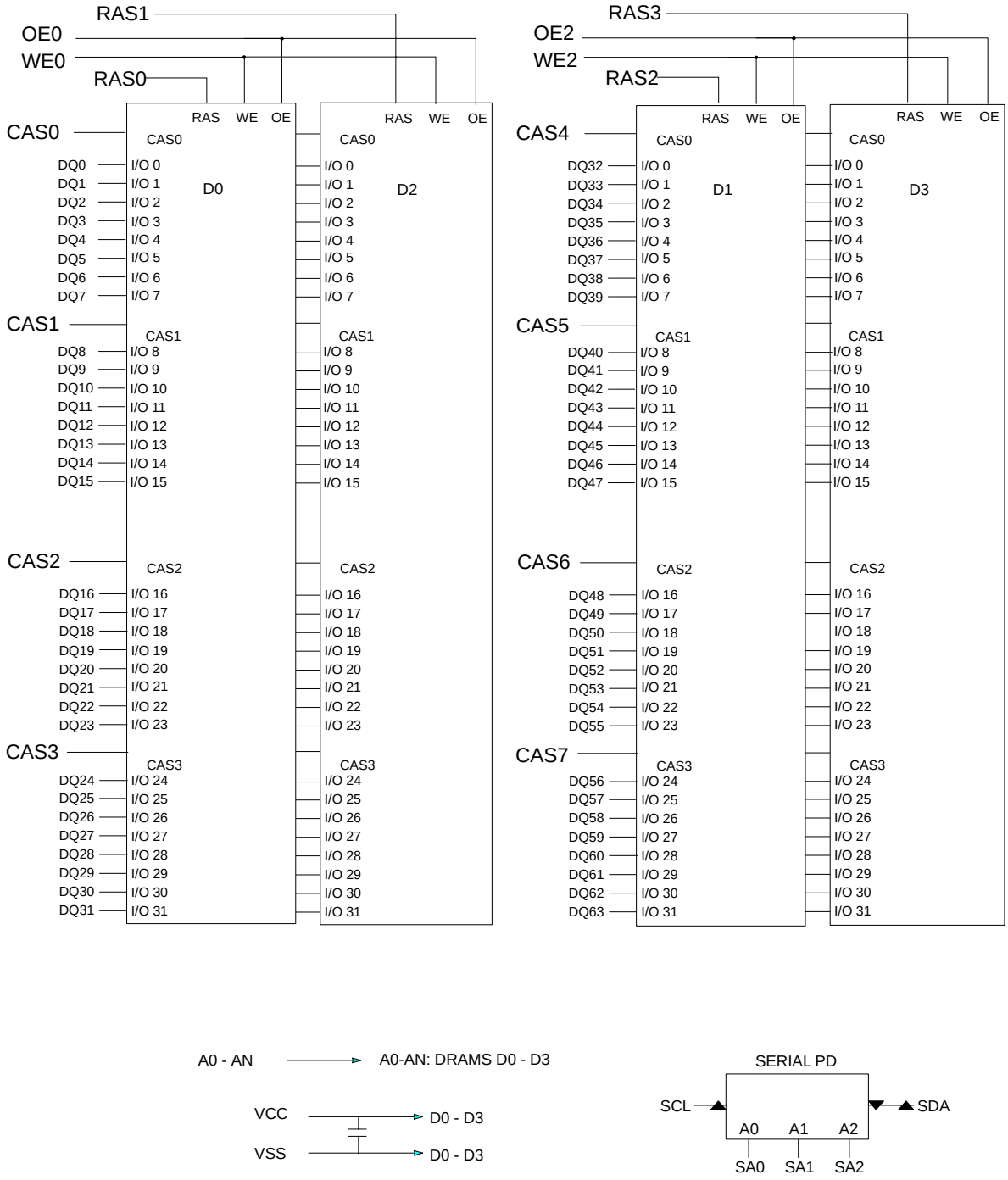


Figure 4.5.3–U
168 Pin X64 DRAM DIMM, 2 BANK, X32 DRAMs