4.4.8 – 100 PIN DRAM, SDRAM & ROM DIMM FAMILY

CAPACITY—up to the addressing capacity of 16 bits, address multiplexed with words of 32, 36, & 40 bits.

DATA CONFIGURATIONS—Seven DATA Word configurations are defined:

—32 BIT DRAM & SDRAM without PARITY
—36 BIT DRAM & SDRAM for ECC CODES
—40 BIT DRAM & SDRAM for ECC CODES
—32 BIT MULTIPLEXED ROM without PARITY.

CONFIGURATION—26 Different Configurations are defined using various combinationa of X1, X4, X8, and X16 DRAM & SDRAM memories including 2 bank configurations, 5 for DRAM and 21 for SDRAM.

LOGIC FEATURES—The modules contain the Serial Presence Detect (SPD) feature that conist of a built in serial access EEPROM that stores information on mutiple parameters and attributes of the module such as technology, storage capacity, configuration, data word configuration, refresh mode, and speed of the module.

PACKAGE—100 PIN JEDEC DIMM MEMORY MODULE

PIN ASSIGNMENTS —Figs. 4.4.8–A & 4.4.8–B

TECHNOLOGY COMPARISON TABLE — Fig. 4.4.8–C

SDRAM CLOCK WIRING DIAGRAMS — Fig. 4.4.8–D

SDRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.4.8–E through 4.4.8–Z

DRAM CONFIGURATION BLOCK DIAGRAMS —Figs. 4.4.8–AA through 4.4.8–AE

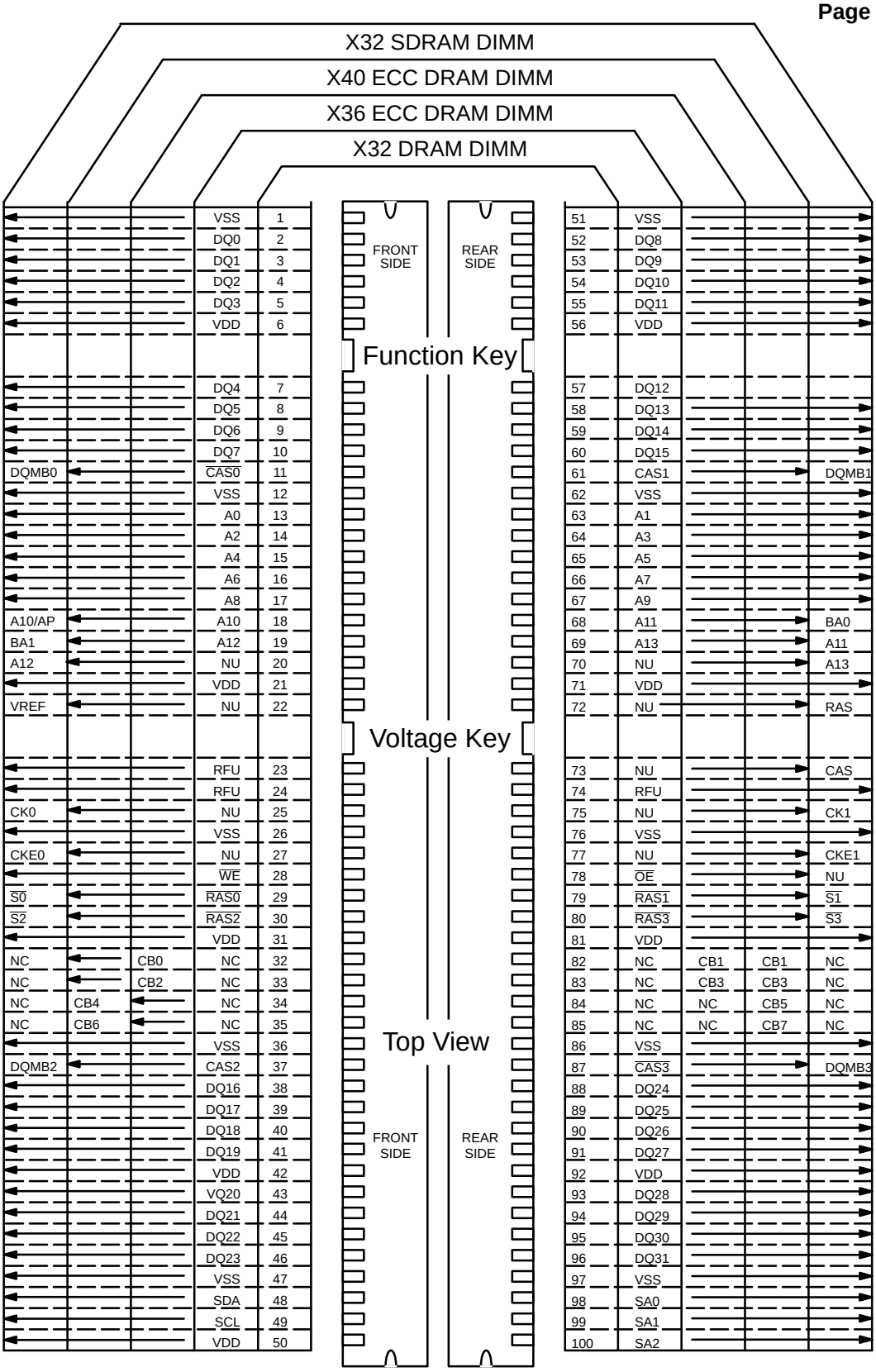


FIGURE 4.4.8– B

100 Pin 32, 36, or 40 BIT DRAM, 32 BIT SDRAM DIMM PINOUT

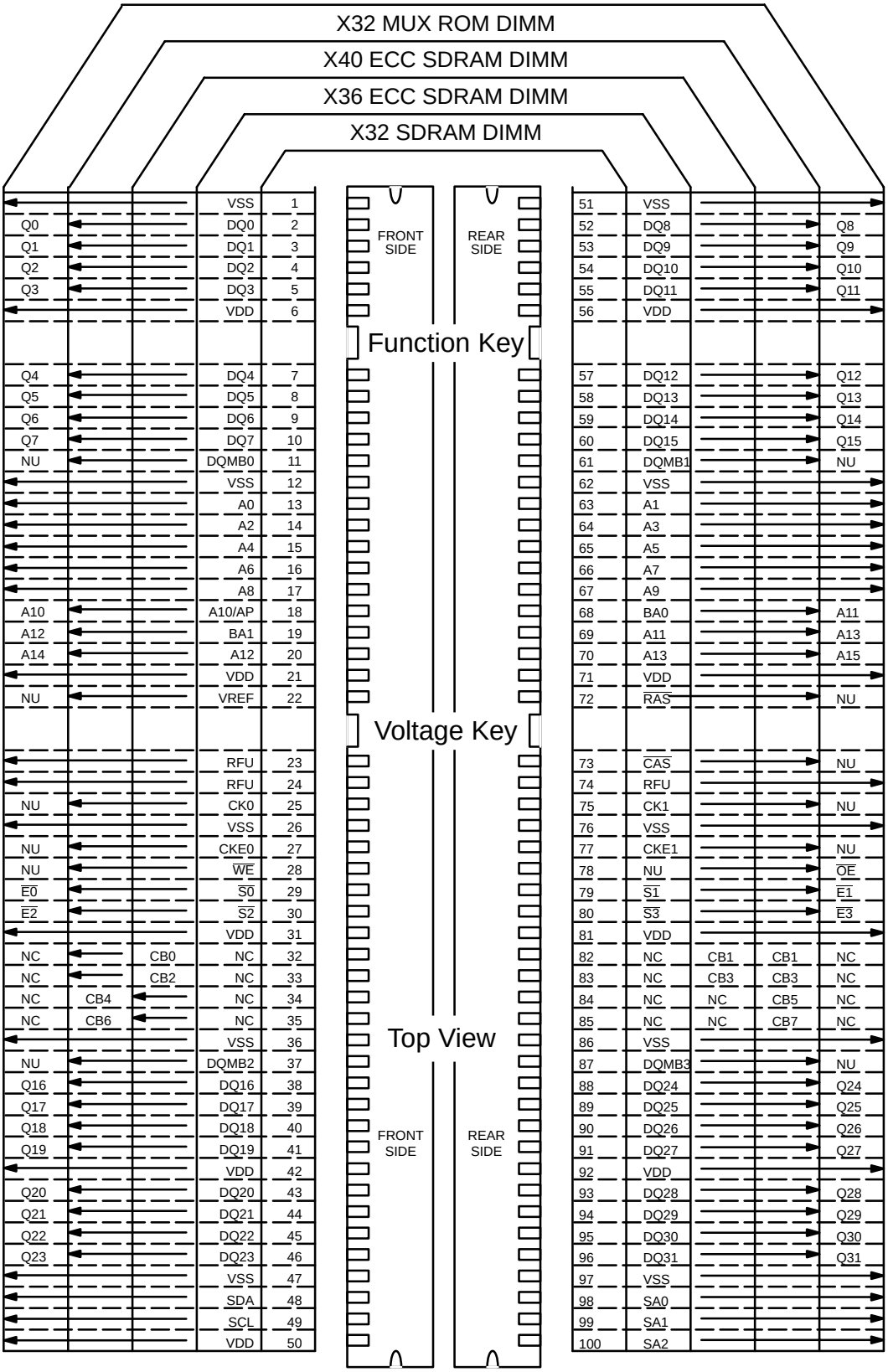


FIGURE 4.4.8– C

100 Pin 32, 36, or 40 BIT DRAM, 32 BIT SDRAM DIMM PINOUT

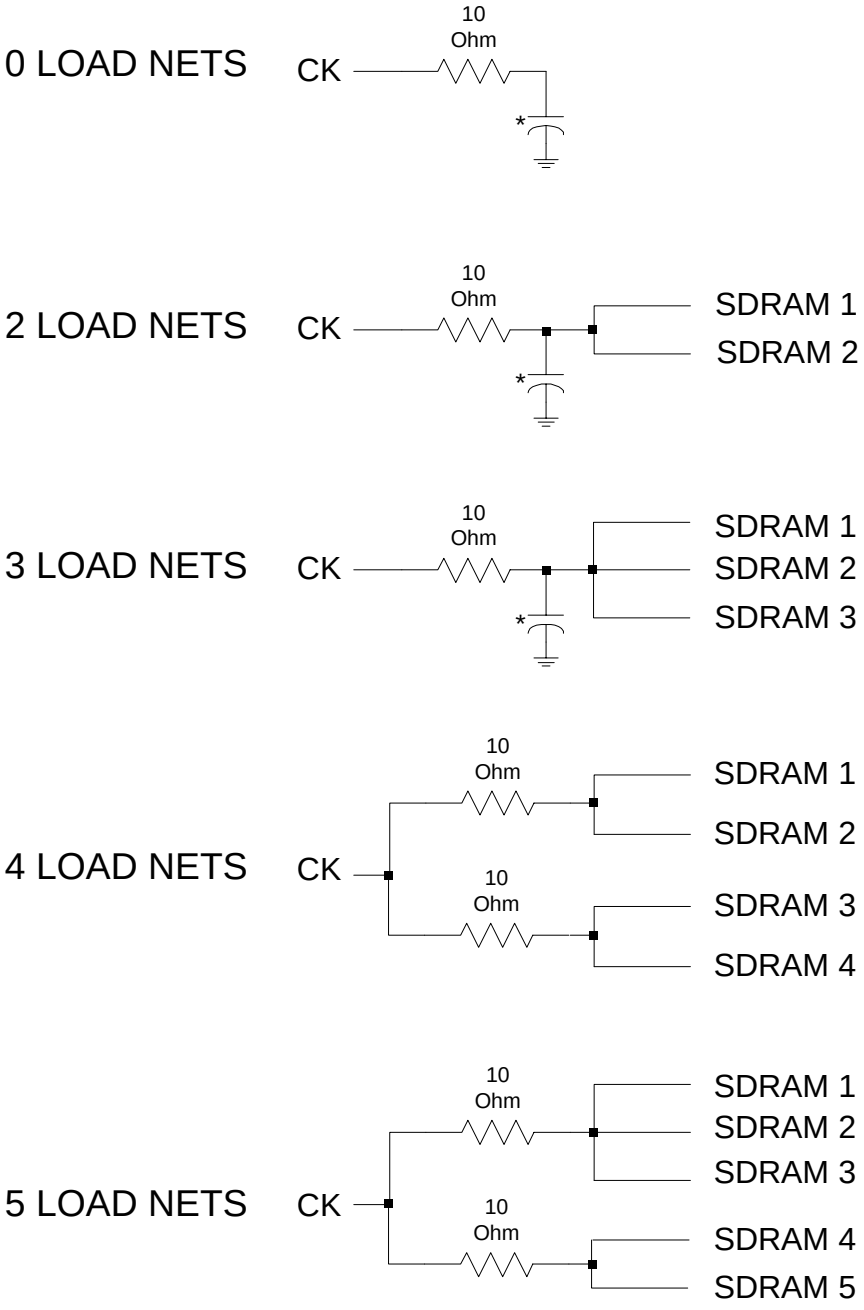
100 PIN DRAM/SDRAM DIMM PINOUT COMPARISON

PIN	DRAM DIMM	SDRAM DIMM	MUX ROM
11	$\overline{CAS0}$	DQMB0	NU
18	A10	A10/AP	A10
19	A12	BA1	A12
20	NU	A12	A14
22	NU	Vref	NU
25	NU	CK0	NU
27	NU	CKE0	NU
28	$\overline{WE}$	$\overline{WE}$	NU
29	$\overline{RAS0}$	$\overline{S0}$	$\overline{E0}$
30	$\overline{RAS2}$	$\overline{S2}$	$\overline{E2}$
37	$\overline{CAS2}$	DQMB2	NU
61	$\overline{CAS1}$	DQMB1	NU
68	A11	BA0	A11
69	A13	A11	A13
70	NU	A13	A15
72	NU	$\overline{RAS}$	NU
73	NU	$\overline{CAS}$	NU
75	NU	CK1	NU
77	NU	CKE1	NU
78	$\overline{OE}$	NU	$\overline{OE}$
79	$\overline{RAS1}$	$\overline{S1}$	$\overline{E1}$
80	$\overline{RAS3}$	$\overline{S3}$	$\overline{E3}$
87	$\overline{CAS3}$	DQMB3	NU

Notes:

1. A10 on DRAM DIMM is also AP on SDRAM DIMM
2. A14 on DRAM DIMM is also BA0 on SDRAM DIMM
3. A15 on DRAM DIMM is also BA1 on SDRAM DIMM (for 4 Bank SDRAM).

Figure 4.4.8–D
100 Pin DRAM, SDRAM, & ROM DIMM, PIN COMPARISON



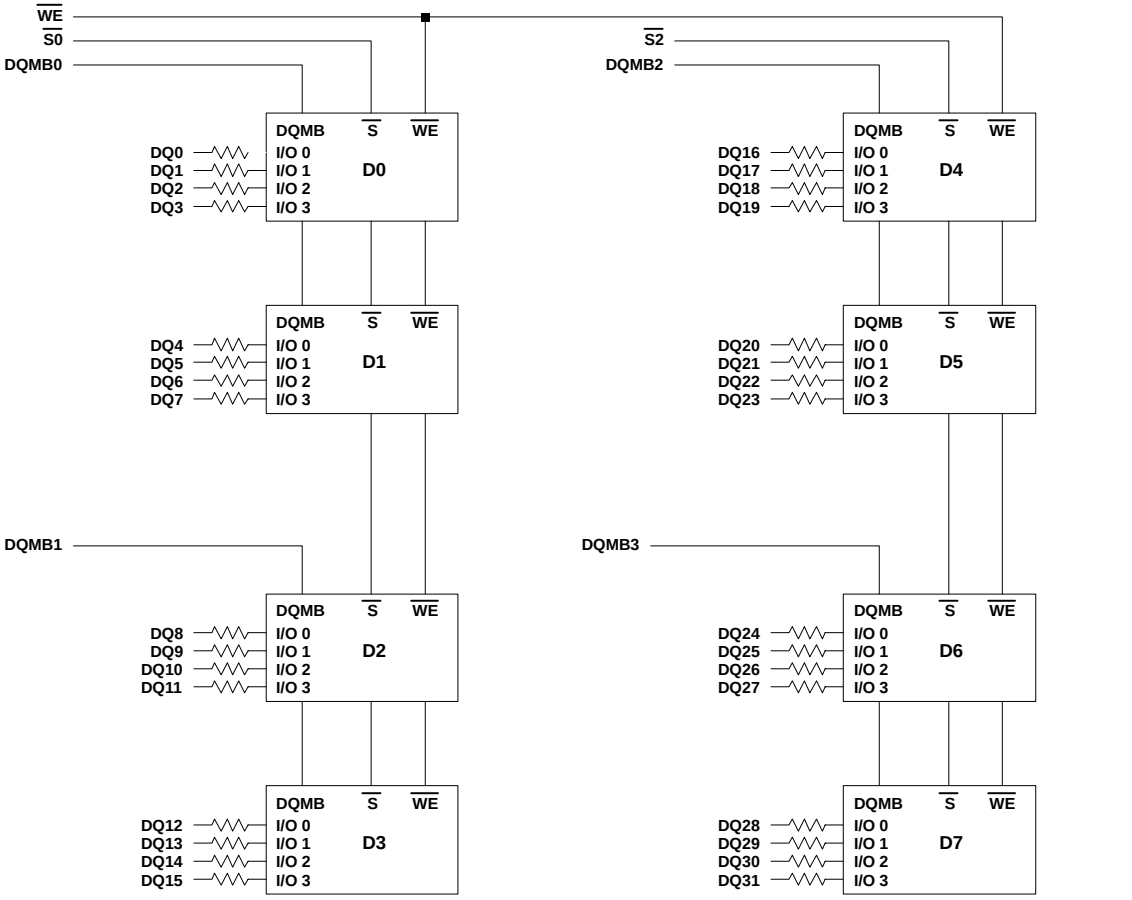
Notes:

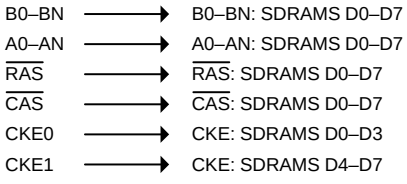
1. THE CK INPUTS SHOULD HAVE A NOMINAL DELAY OF .4ns MEASURED FROM THE CK INPUT AT THE DIMM TAB TO THE CK INPUT OF THE SDRAM (OR PADDING CAPACITOR). (EG: THIS IS APPROXIMATELY 2" OF PCB WIRE AND 2.5pf OF INPUT CAPACITANCE).

2.) THE VARIATION OF CK INPUT DELAY WILL BE +/– .1NS FOR BOTH CK INPUTS. (EG: IF THE WIRE IMPEDANCE IS APPROX. 65 ohms, THIS CORRESPONDS TO A CAPACITANCE VARIATION OF +/– 3pf IN TOTAL CK INPUT CAPACITANCE).

* NOTE: Add padding capacitor to make the capacitance equal that of 4 loads total.

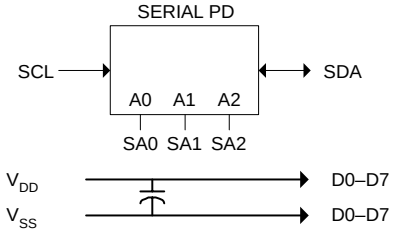
Figure 4.4.8–E
100 Pin SDRAM DIMM, CLOCK WIRING





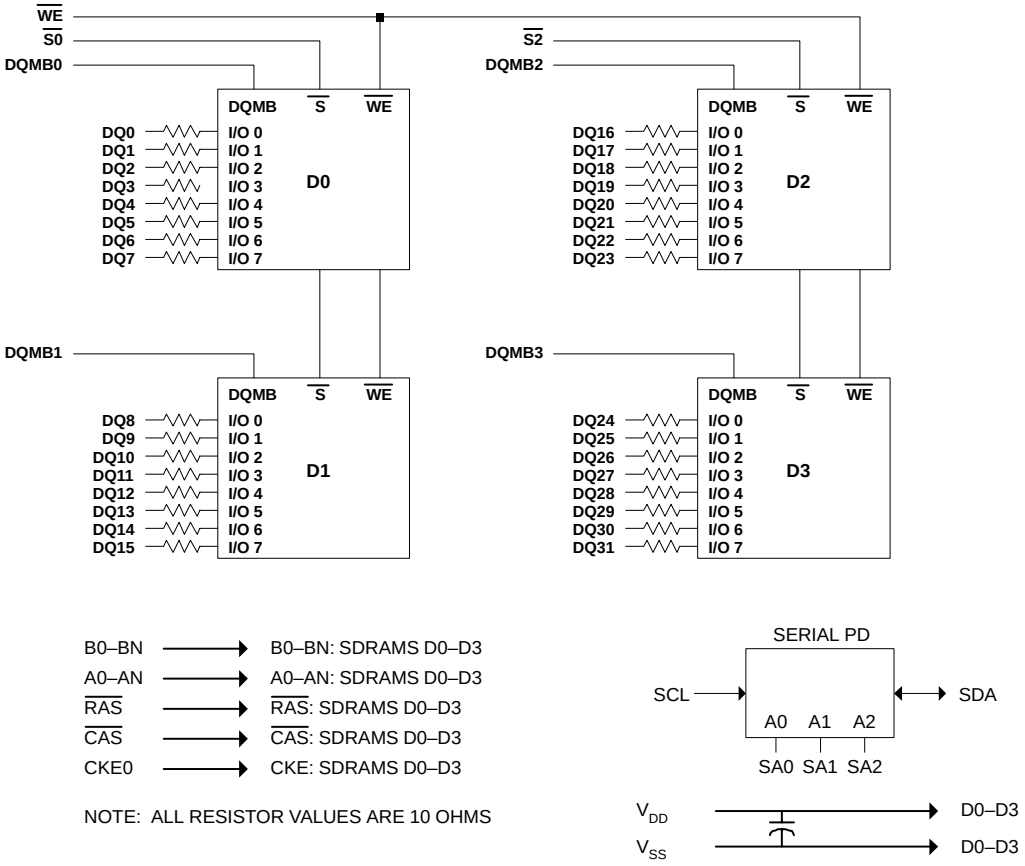
Clock Wiring	
Clock Input	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams



NOTE: ALL RESISTOR VALUES ARE 10 OHMS

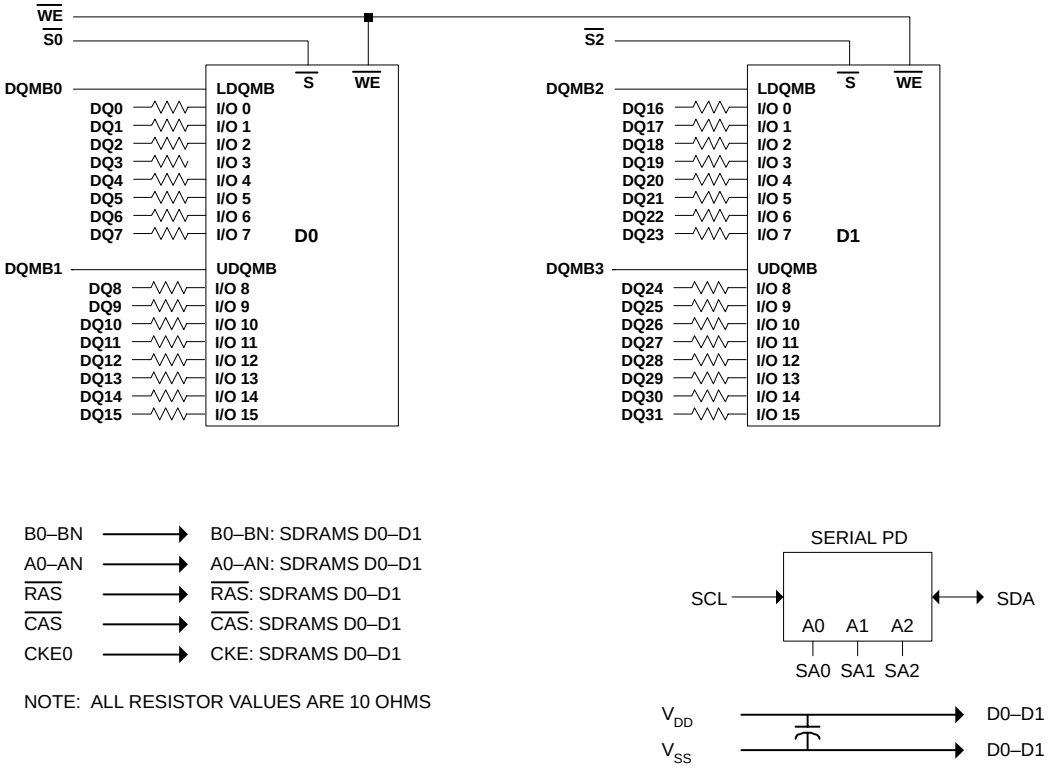
Figure 4.4.8–F
100 Pin X32 SDRAM DIMM, 1 Bank with X4 SDRAMs



Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	4 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–G
100 Pin X32 SDRAM DIMM, 1 Bank with X8 SDRAMs

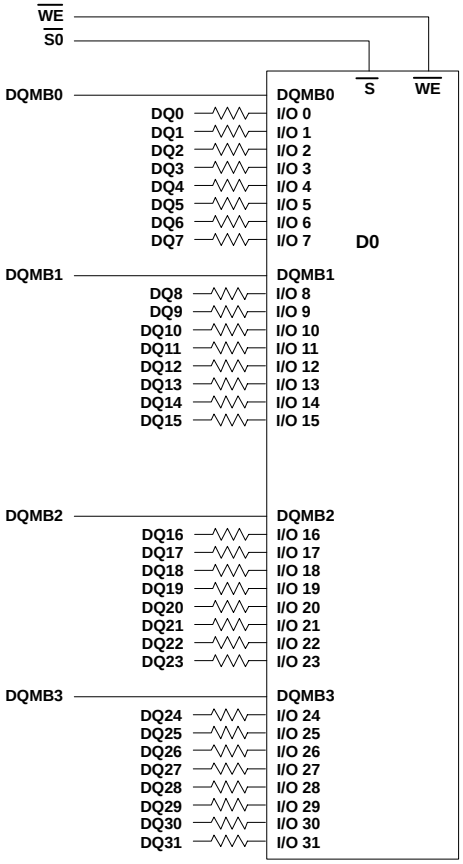


NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	2 SDRAMS

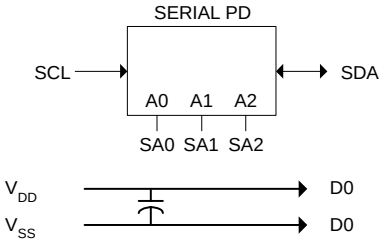
*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–H
100 Pin X32 SDRAM DIMM, 1 Bank with X16 SDRAMs



B0–BN → B0–BN: SDRAMS D0
A0–AN → A0–AN: SDRAMS D0
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0
CKE0 → CKE: SDRAMS D0

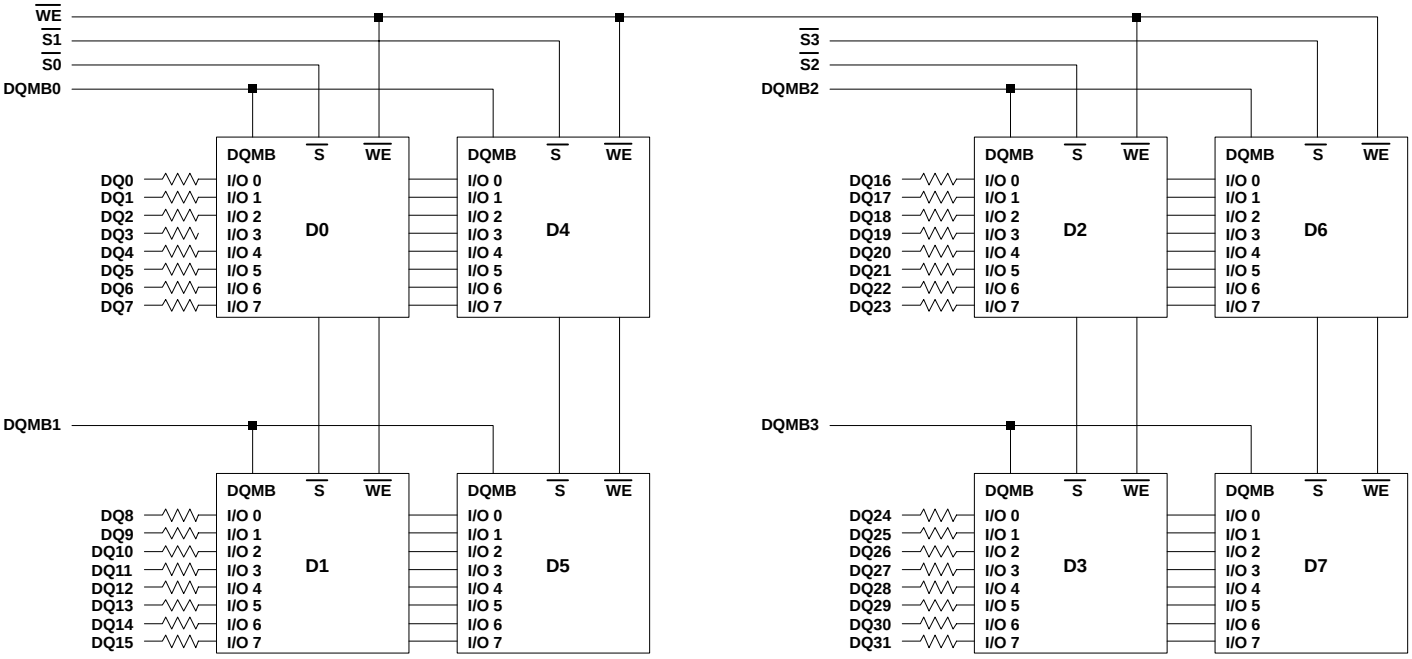
NOTE: ALL RESISTOR VALUES ARE 10 OHMS



Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	1 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–I
100 Pin X32 SDRAM DIMM, 1 Bank with X32 SDRAMs



B0–BN → B0–BN: SDRAMS D0–D7
A0–AN → A0–AN: SDRAMS D0–D7
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D7
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D7
CKE0 → CKE: SDRAMS D0–D3
CKE1 → CKE: SDRAMS D4–D7

NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0	4 SDRAMS
*CK1	4 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

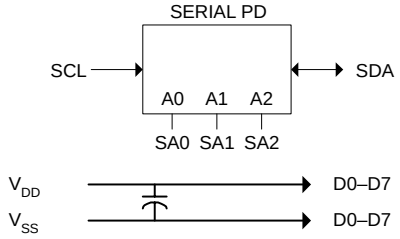
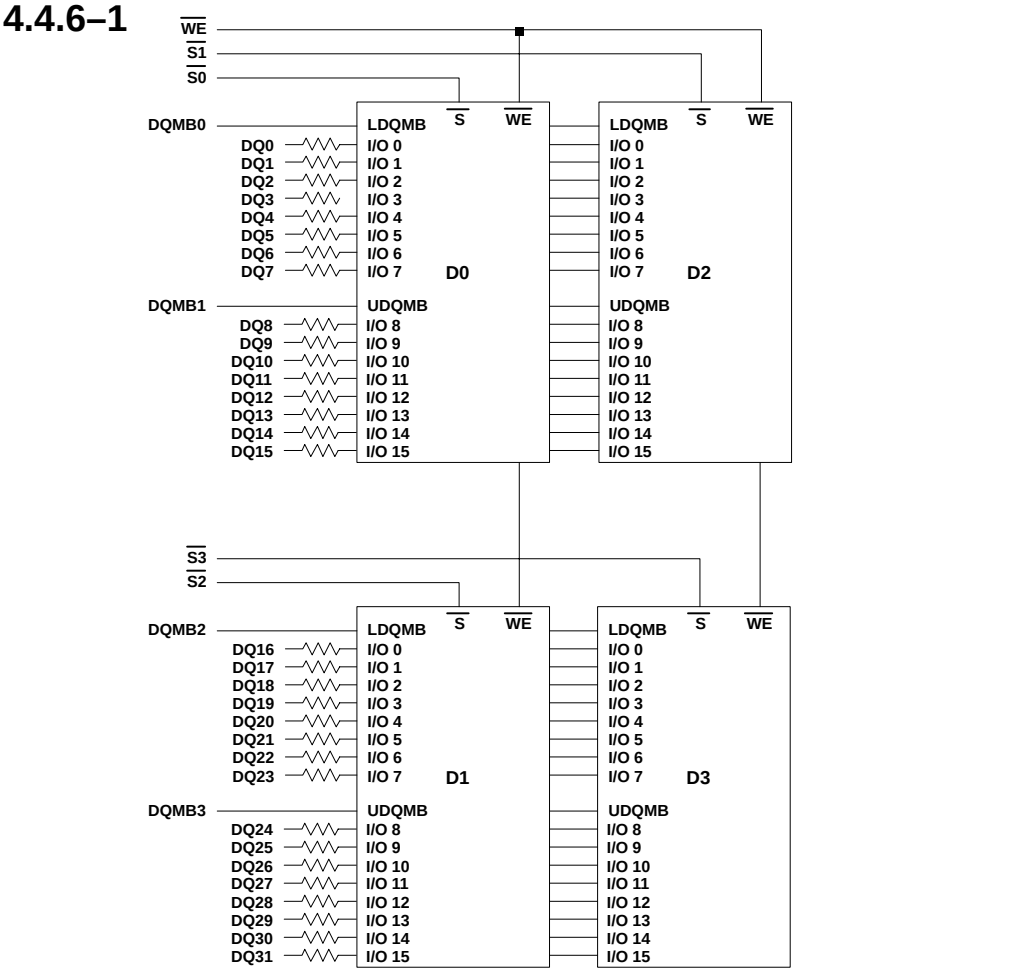
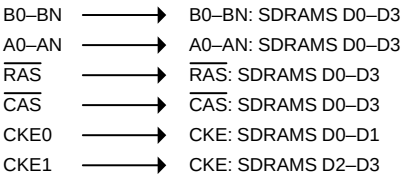


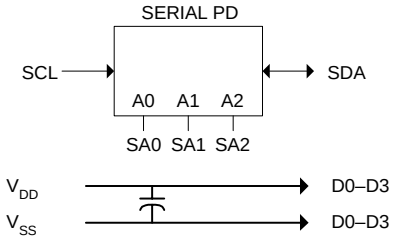
Figure 4.4.8–J
100 Pin X32 SDRAM DIMM, 2 Bank with X8 SDRAMs

4.4.6–1





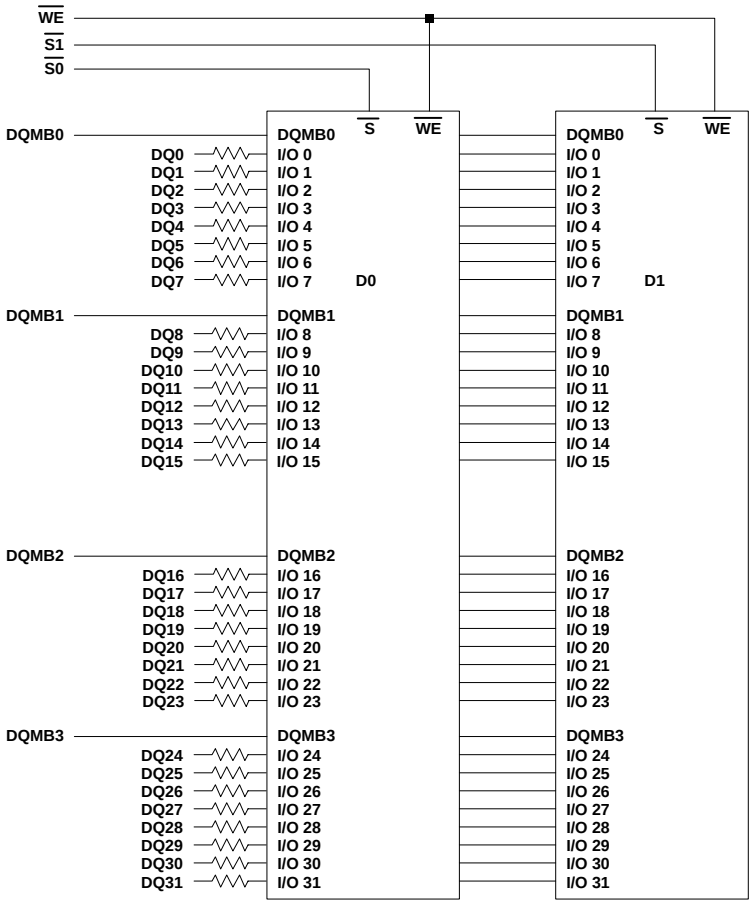
NOTE: ALL RESISTOR VALUES ARE 10 OHMS



Clock Wiring	
Clock Input	SDRAMS
*CK0	2 SDRAMS
*CK1	2 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–K
100 Pin X32 SDRAM DIMM, 2 Bank with X16 SDRAMs



B0–BN → B0–BN: SDRAMS D0–D1

A0–AN → A0–AN: SDRAMS D0–D1

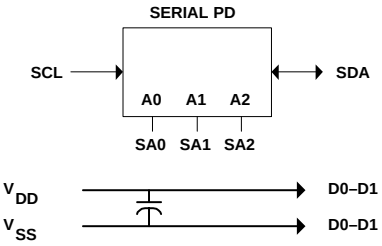
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D1

$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D1

CKE0 → CKE: SDRAMS D0

CKE1 → CKE: SDRAMS D1

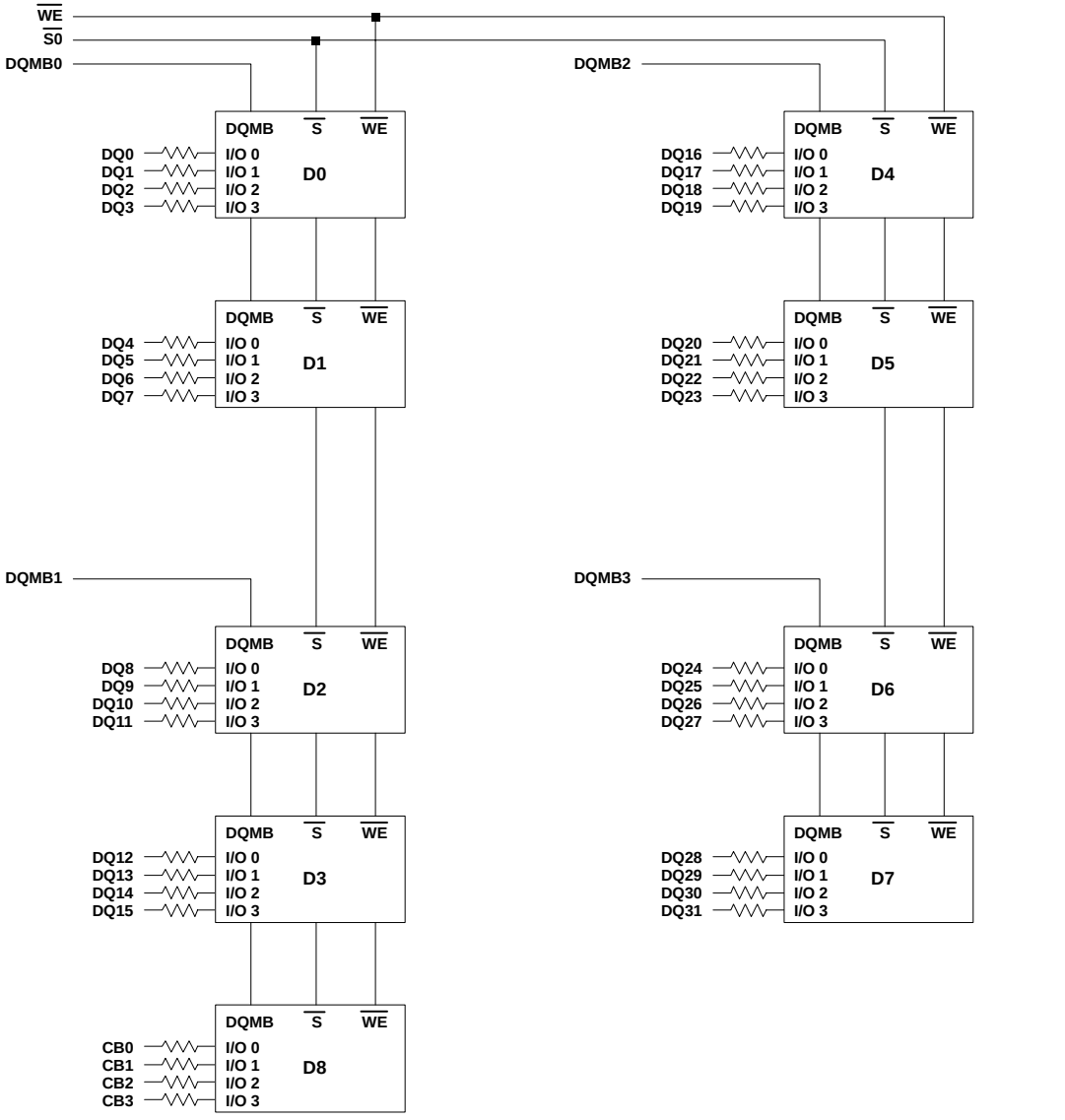
NOTE: ALL RESISTOR VALUES ARE 10 OHMS



Clock Wiring	
Clock Input	SDRAMS
*CK0	1 SDRAM
*CK1	1 SDRAM

*Wire per Clock Loading Table/Wiring Diagrams

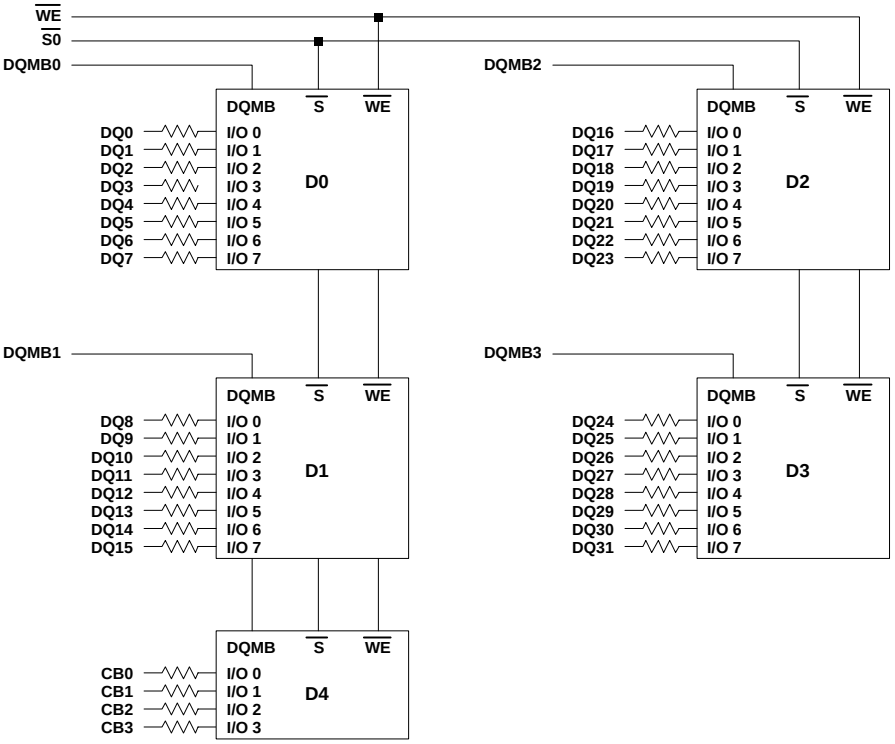
Figure 4.4.8–L
100 Pin X32 SDRAM DIMM, 2 Bank with X32 SDRAMs

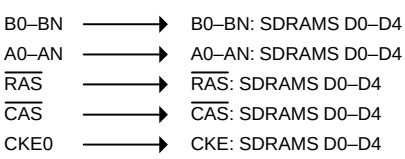


Clock Wiring	
Clock Input	SDRAMS
*CK0	4 or 5 SDRAMS
*CK1	4 or 5 SDRAMS

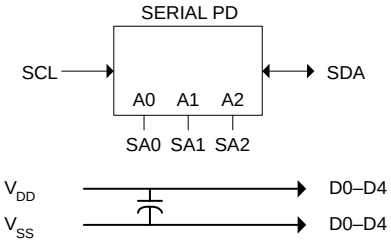
*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–M
100 Pin X36 ECC SDRAM DIMM, 1 Bank with X4 SDRAMs





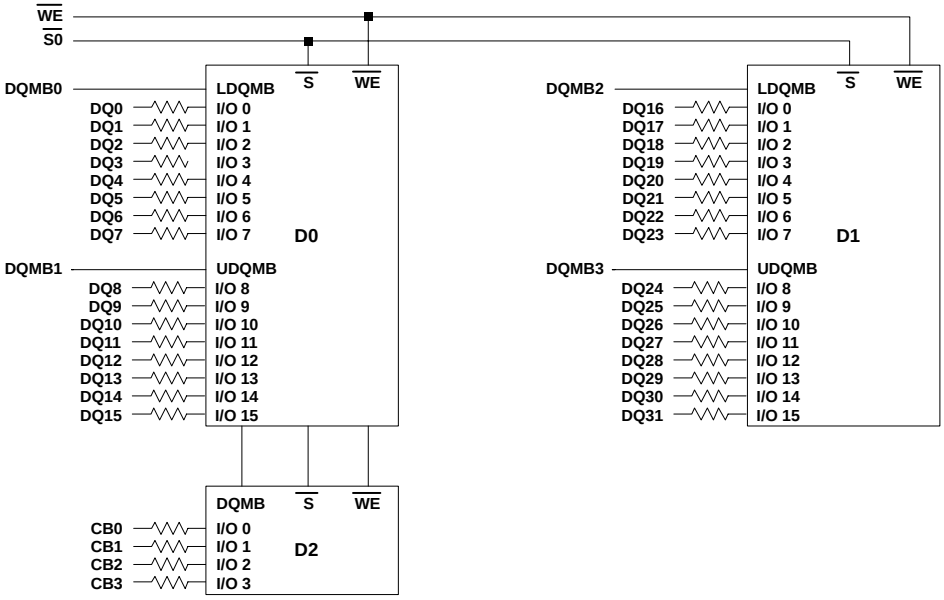
NOTE: ALL RESISTOR VALUES ARE 10 OHMS

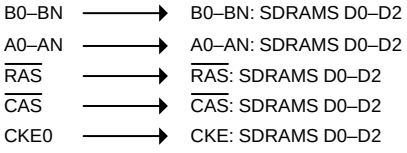


Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	5 SDRAMS

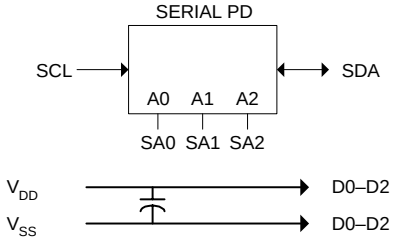
*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–N
100 Pin X36 ECC SDRAM DIMM, 1 Bank with X4 & X8 SDRAMs





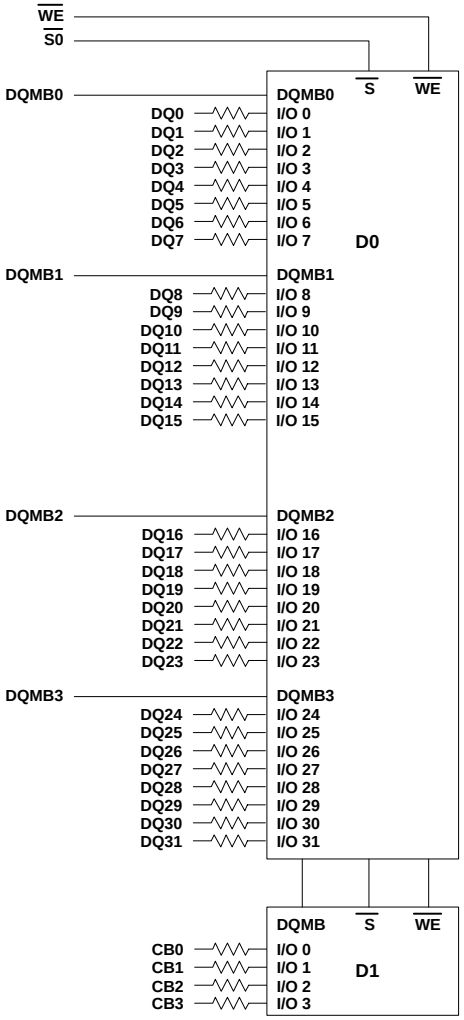
NOTE: ALL RESISTOR VALUES ARE 10 OHMS



Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	3 SDRAMS

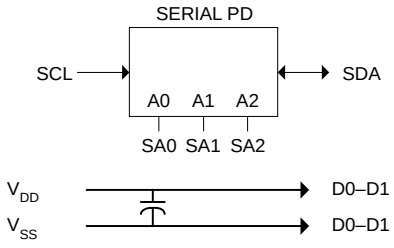
*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–O
100 Pin X36 ECC SDRAM DIMM, 1 Bank with X4 & X16 SDRAMs



B0–BN → B0–BN: SDRAMS D0–D1
A0–AN → A0–AN: SDRAMS D0–D1
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D1
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D1
CKE0 → CKE: SDRAMS D0–D1

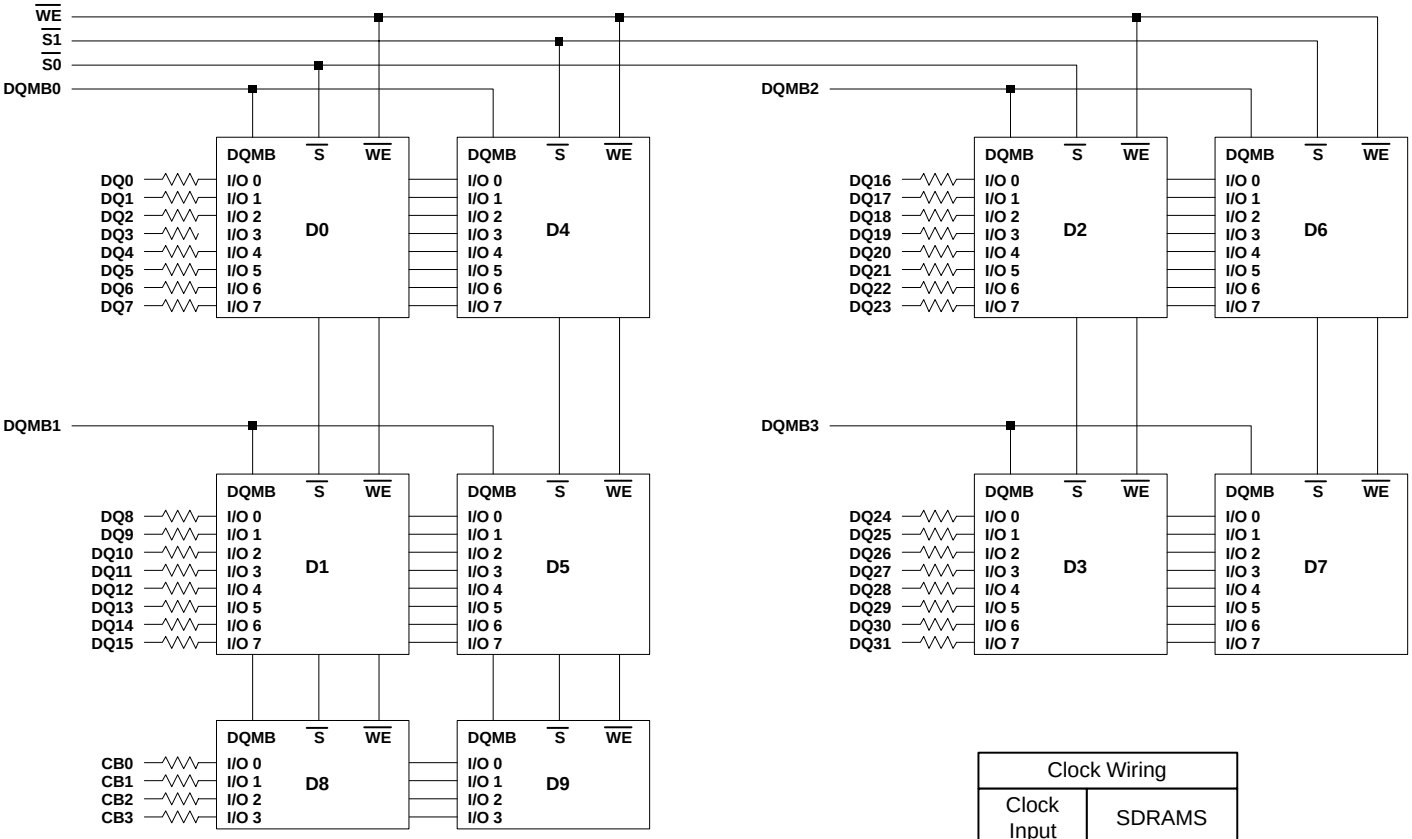
NOTE: ALL RESISTOR VALUES ARE 10 OHMS



Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	2 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–P
100 Pin X36 ECC SDRAM DIMM, 1 Bank with X4 & X32 SDRAMs



Clock Wiring	
Clock Input	SDRAMS
*CK0	5 SDRAMS
*CK1	5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

B0–BN → B0–BN: SDRAMS D0–D9
A0–AN → A0–AN: SDRAMS D0–D9
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D9
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D9
CKE0 → CKE: SDRAMS D0–D3, D8
CKE1 → CKE: SDRAMS D4–D7, D9

NOTE: ALL RESISTOR VALUES ARE 10 OHMS

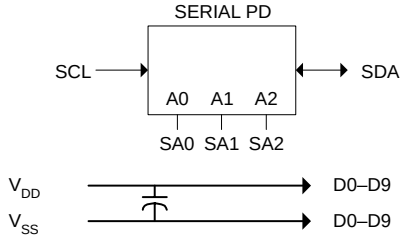
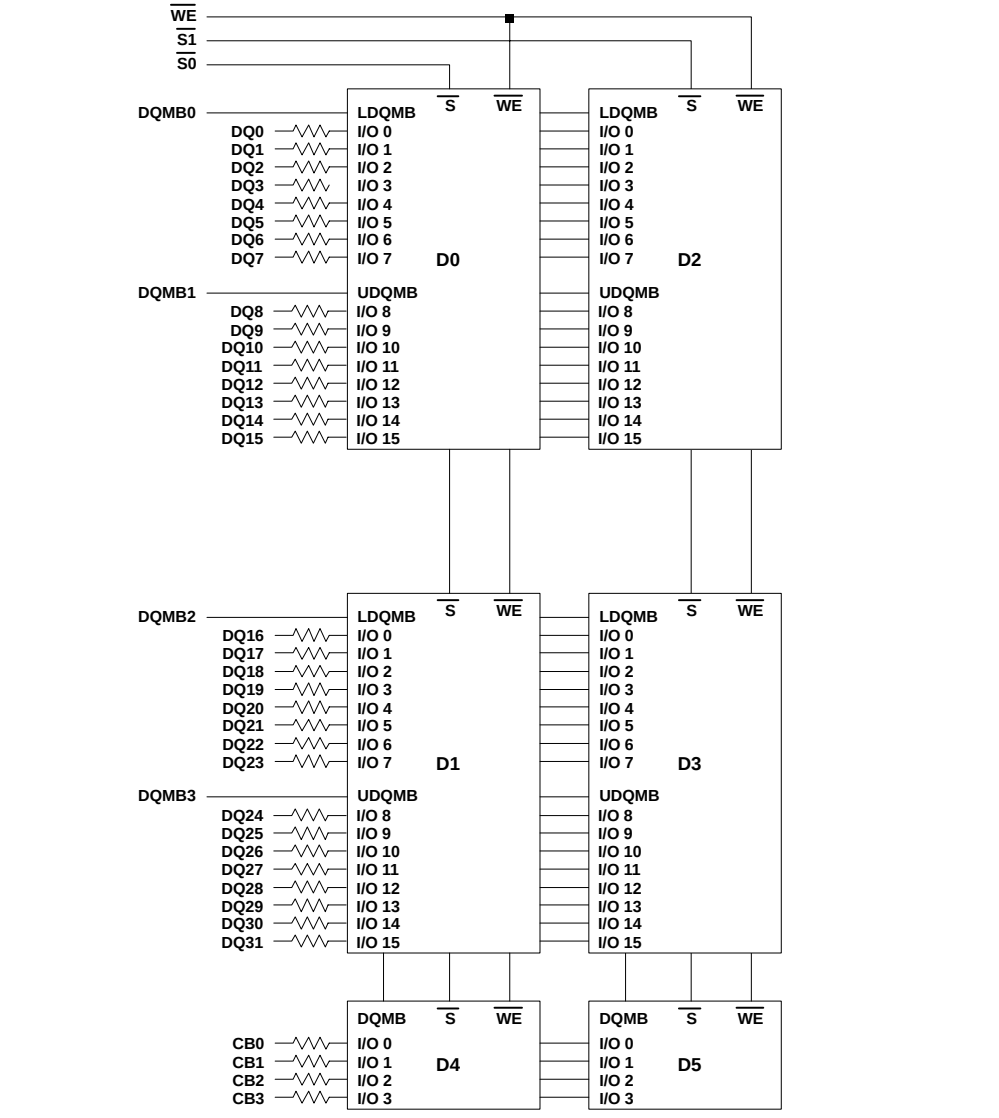
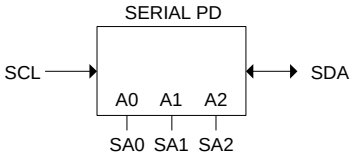


Figure 4.4.8–Q
100 Pin X36 ECC SDRAM DIMM, 2 Bank with X4 & X8 SDRAMs



B0–BN → B0–BN: SDRAMS D0–D5
A0–AN → A0–AN: SDRAMS D0–D5
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D5
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D5
CKE0 → CKE: SDRAMS D0–D1, D4
CKE1 → CKE: SDRAMS D2–D3, D5



NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0	3 SDRAMS
*CK1	3 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

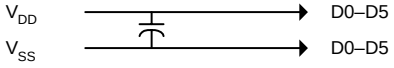
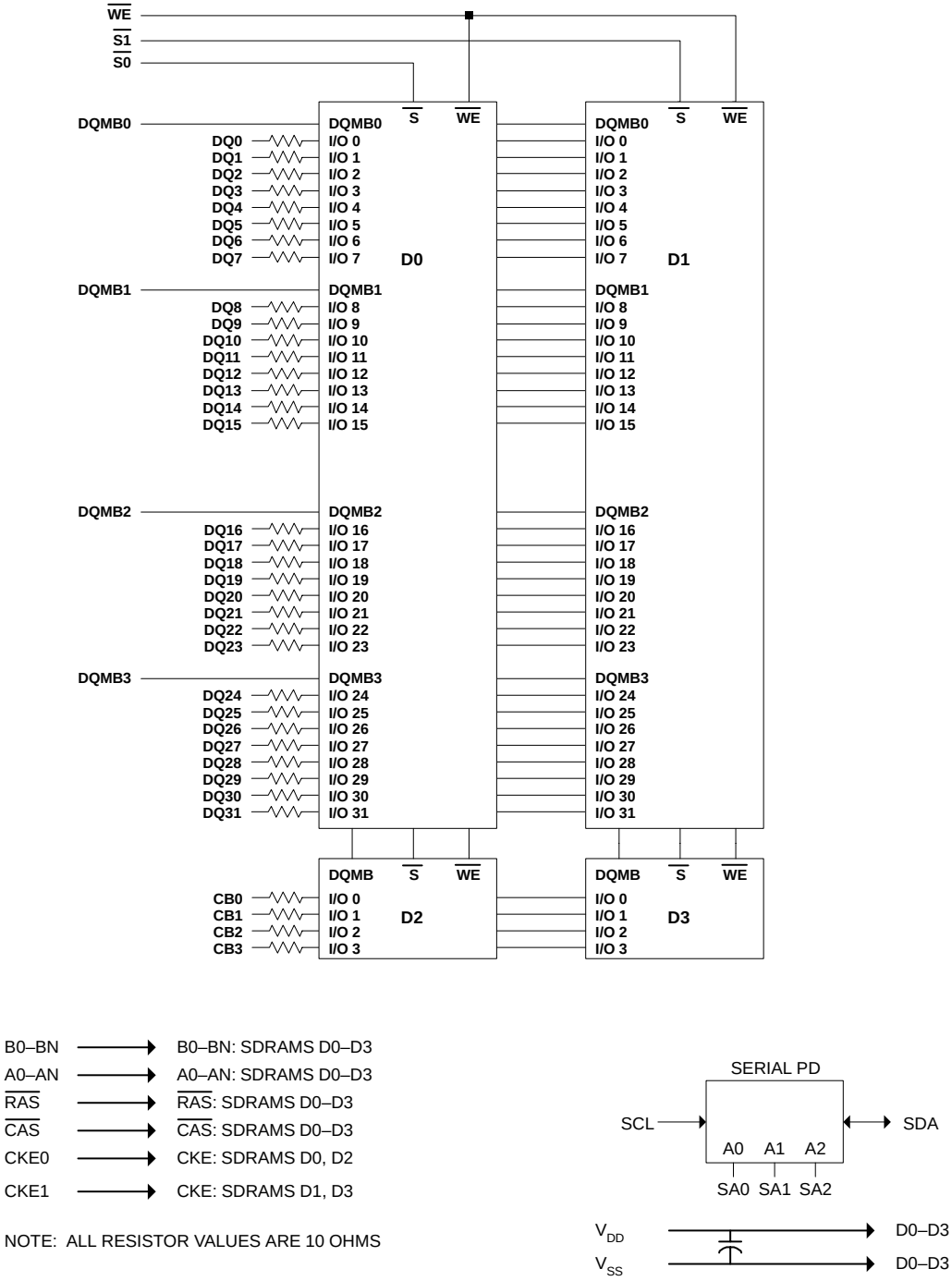


Figure 4.4.8–R
100 Pin X36 ECC SDRAM DIMM, 2 Bank with X4 & X16 SDRAMs



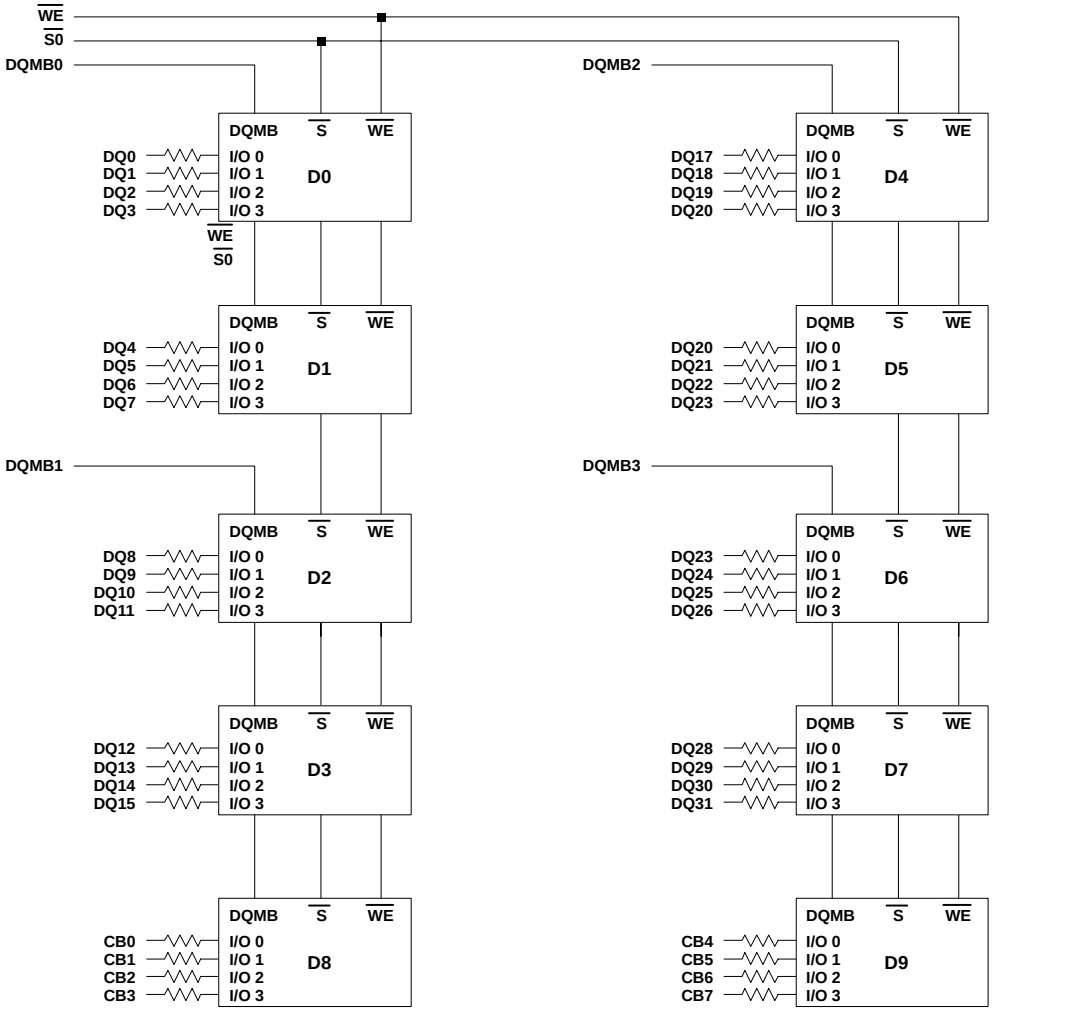
B0–BN → B0–BN: SDRAMS D0–D3
A0–AN → A0–AN: SDRAMS D0–D3
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D3
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D3
CKE0 → CKE: SDRAMS D0, D2
CKE1 → CKE: SDRAMS D1, D3

NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0	2 SDRAMS
*CK1	2 SDRAMS

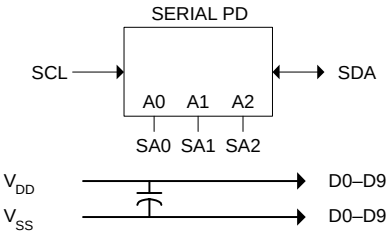
*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–S
100 Pin X36 ECC SDRAM DIMM, 2 Bank with X4 & X32 SDRAMs



B0–BN → B0–BN: SDRAMS D0–D9
A0–AN → A0–AN: SDRAMS D0–D9
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D9
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D9
CKE0 → CKE: SDRAMS D0–D3, D8
CKE1 → CKE: SDRAMS D4–D7, D9

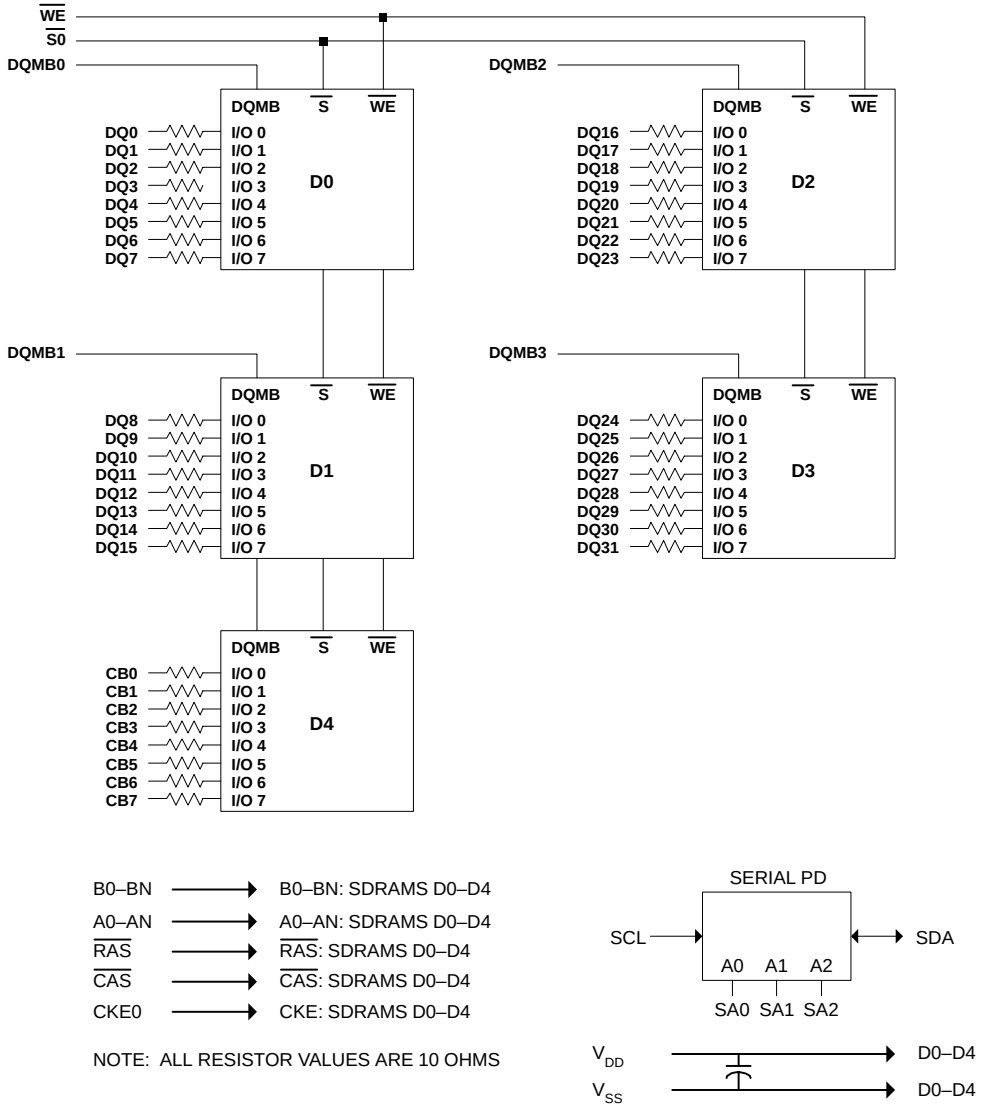
NOTE: ALL RESISTOR VALUES ARE 10 OHMS



Clock Wiring	
Clock Input	SDRAMS
*CK0	5 SDRAMS
*CK1	5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–T
100 Pin X40 ECC SDRAM DIMM, 1 Bank with X4 SDRAMs



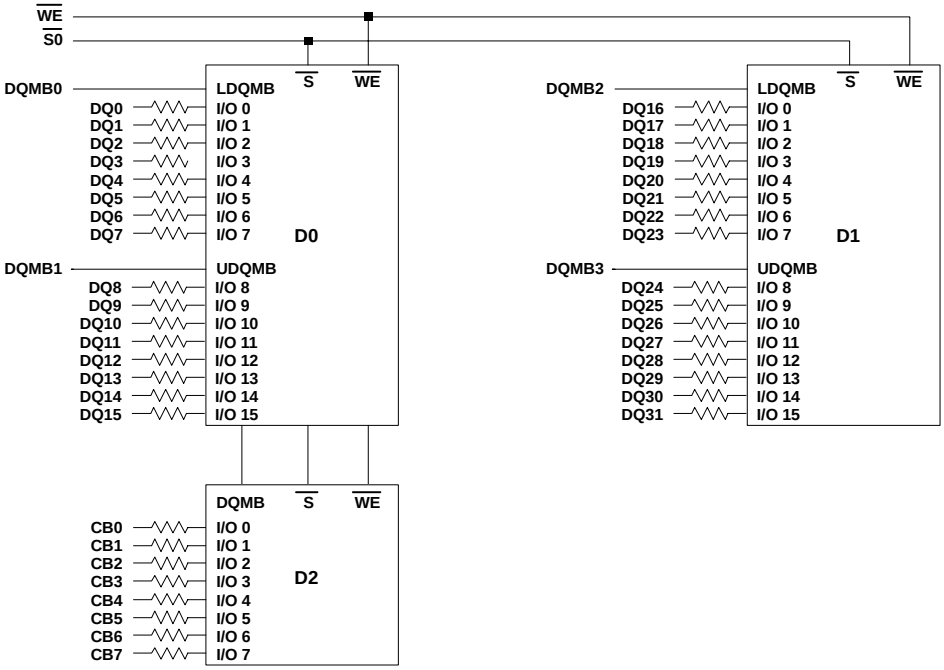
B0–BN → B0–BN: SDRAMS D0–D4
A0–AN → A0–AN: SDRAMS D0–D4
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D4
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D4
CKE0 → CKE: SDRAMS D0–D4

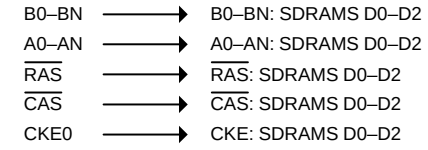
NOTE: ALL RESISTOR VALUES ARE 10 OHMS

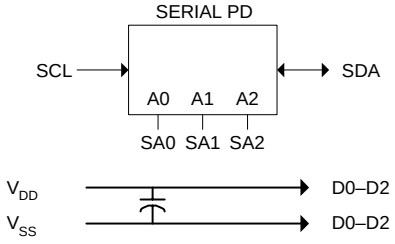
Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–U
100 Pin X40 ECC SDRAM DIMM, 1 Bank with X8 SDRAMs





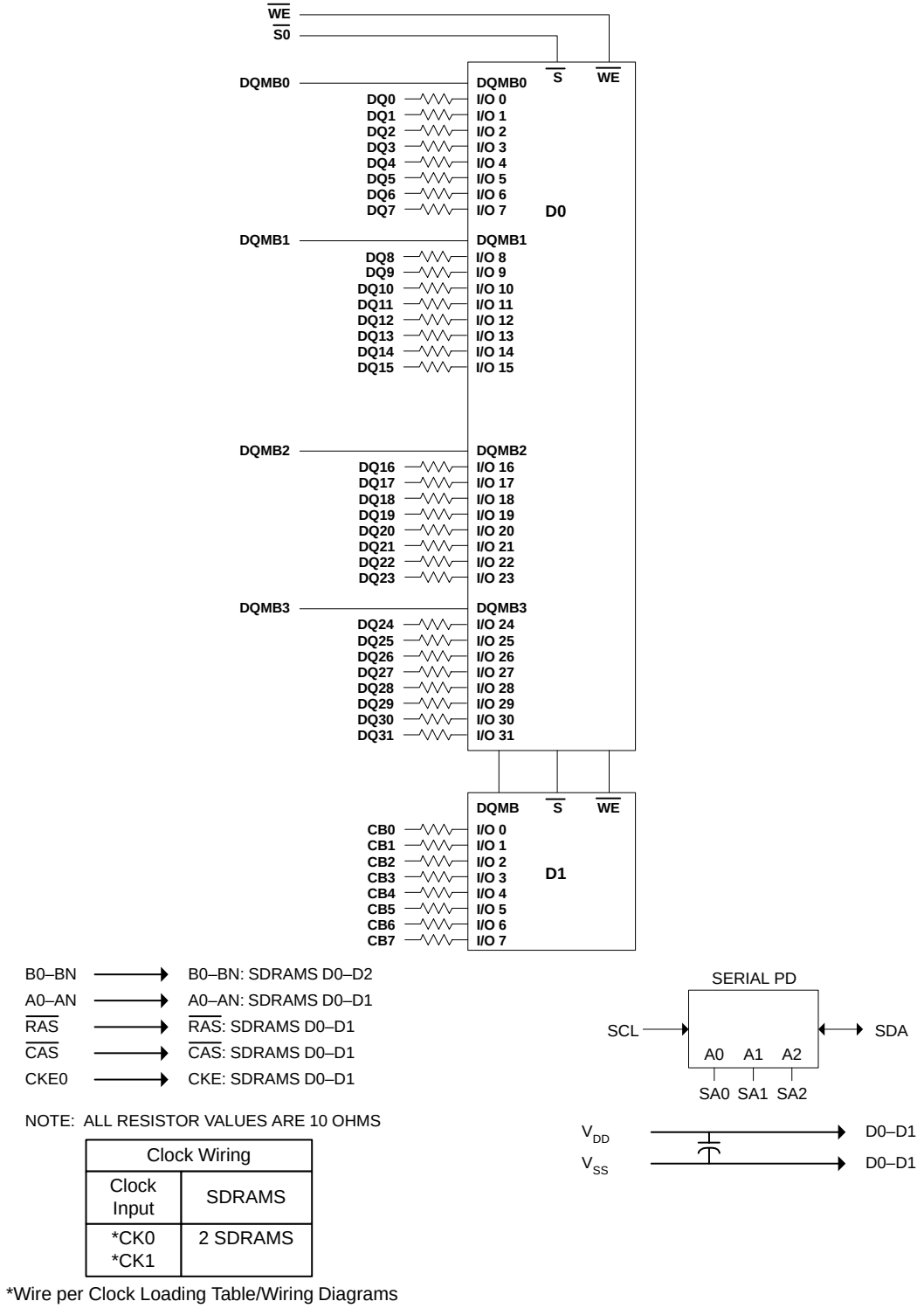


NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	3 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–V
100 Pin X40 ECC SDRAM DIMM, 1 Bank with X8 & X16 SDRAMs

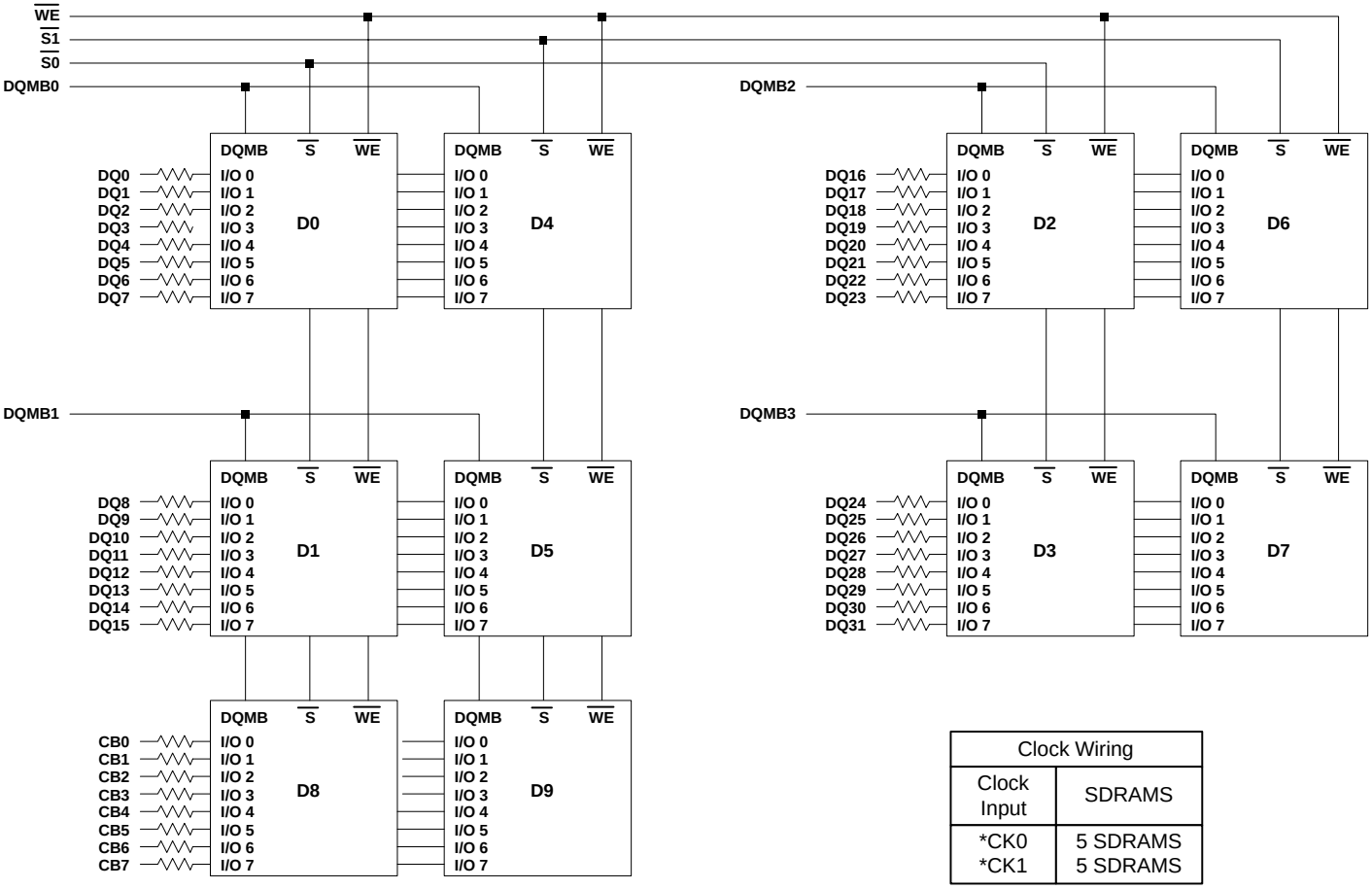


NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0 *CK1	2 SDRAMS

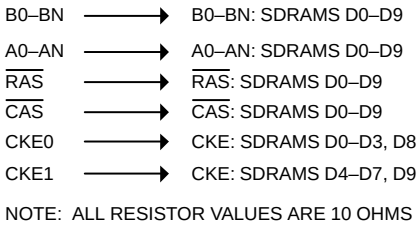
*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–W
100 Pin X40 ECC SDRAM DIMM, 1 Bank with X8 & X32 SDRAMs



Clock Wiring	
Clock Input	SDRAMS
*CK0	5 SDRAMS
*CK1	5 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams



NOTE: ALL RESISTOR VALUES ARE 10 OHMS

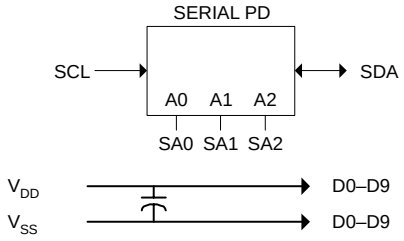
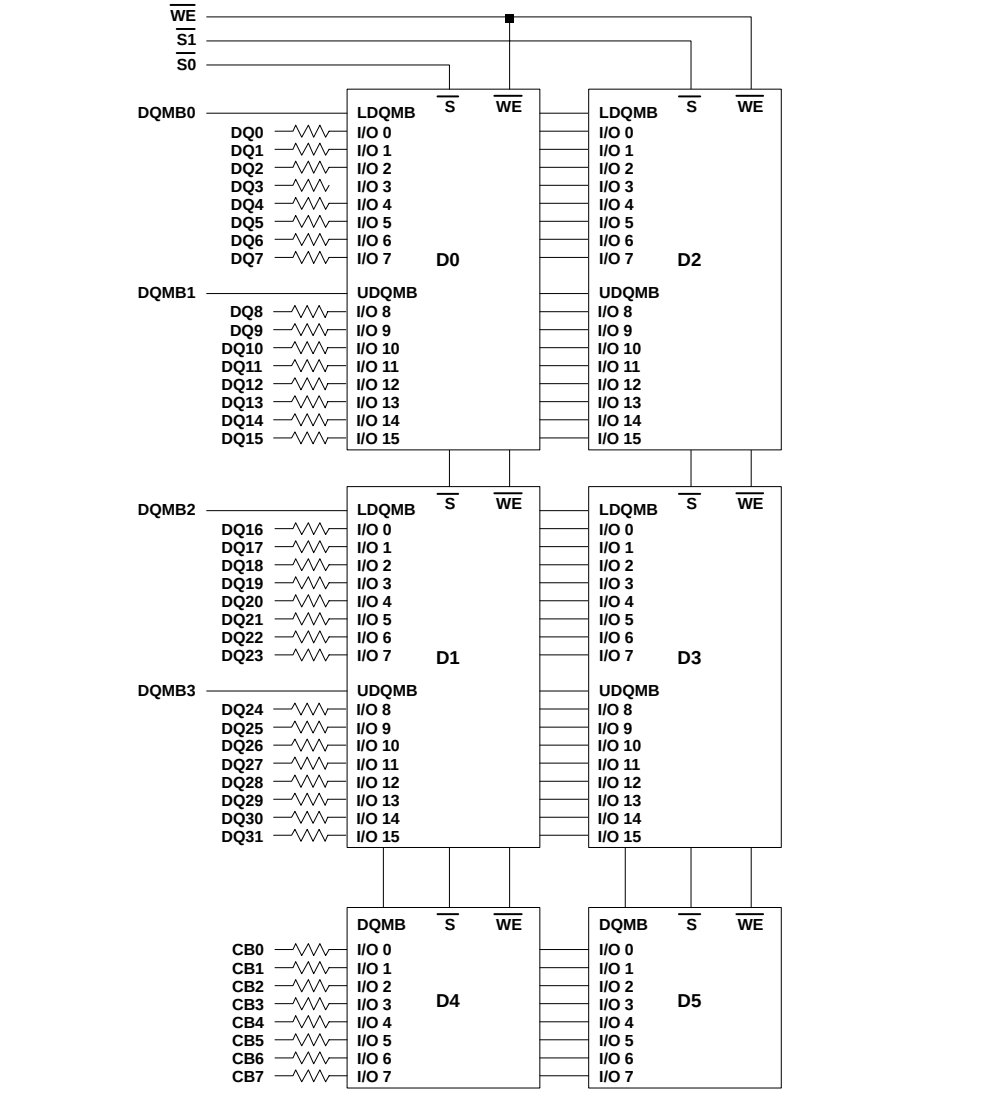
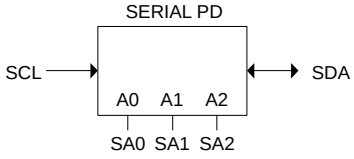


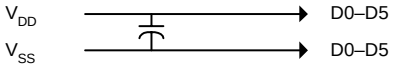
Figure 4.4.8–X
100 Pin X40 ECC SDRAM DIMM, 2 Bank with X8 SDRAMs



B0–BN → B0–BN: SDRAMS D0–D5
A0–AN → A0–AN: SDRAMS D0–D5
$\overline{RAS}$ → $\overline{RAS}$: SDRAMS D0–D5
$\overline{CAS}$ → $\overline{CAS}$: SDRAMS D0–D5
CKE0 → CKE: SDRAMS D0–D1, D4
CKE1 → CKE: SDRAMS D2–D3, D5



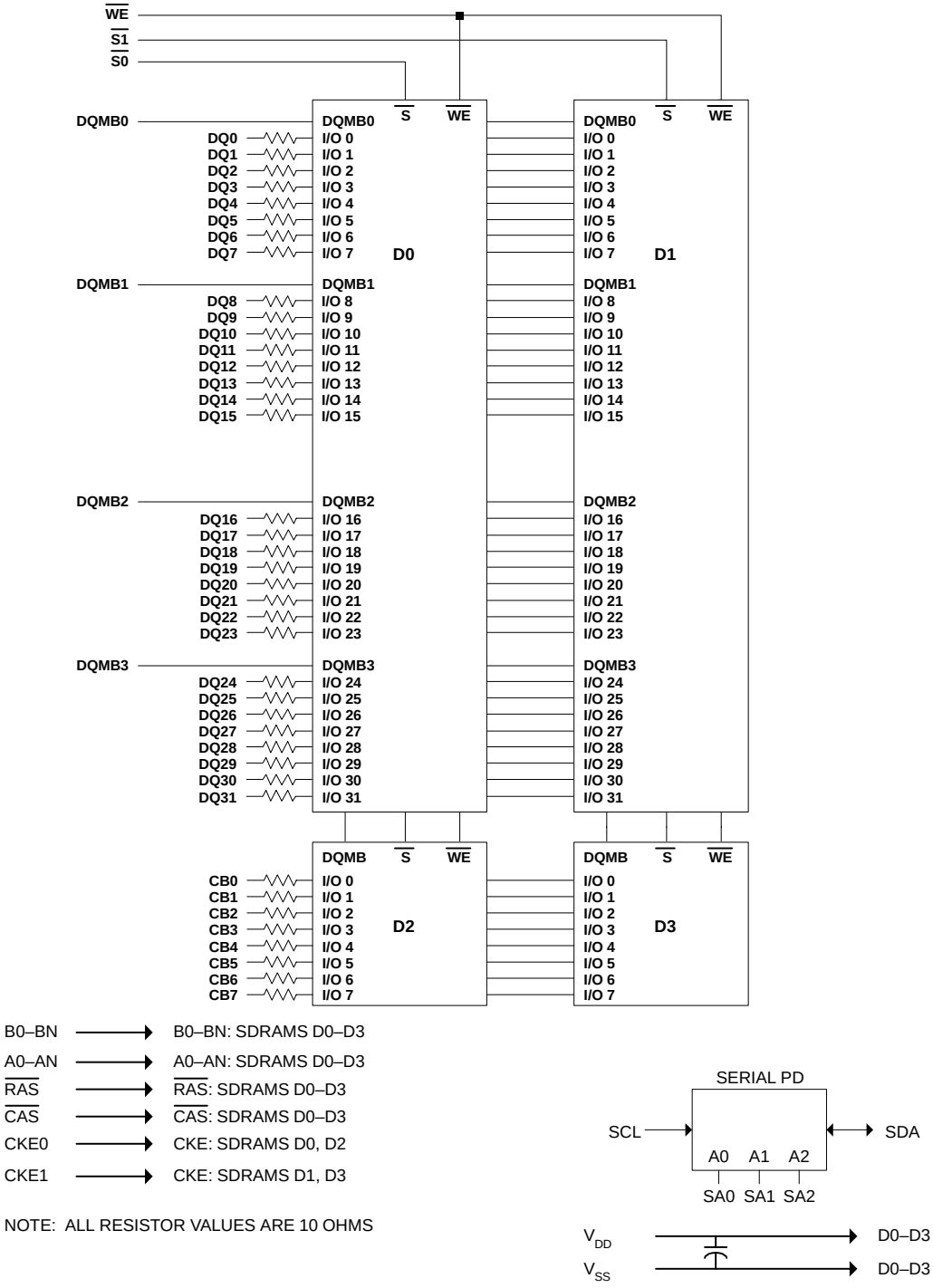
NOTE: ALL RESISTOR VALUES ARE 10 OHMS



Clock Wiring	
Clock Input	SDRAMS
*CK0	3 SDRAMS
*CK1	3 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–Y
100 Pin X40 ECC SDRAM DIMM, 2 Bank with X8 & X16 SDRAMs



NOTE: ALL RESISTOR VALUES ARE 10 OHMS

Clock Wiring	
Clock Input	SDRAMS
*CK0	2 SDRAMS
*CK1	2 SDRAMS

*Wire per Clock Loading Table/Wiring Diagrams

Figure 4.4.8–Z
100 Pin X40 ECC SDRAM DIMM, 2 Bank with X8 & X32 SDRAMs

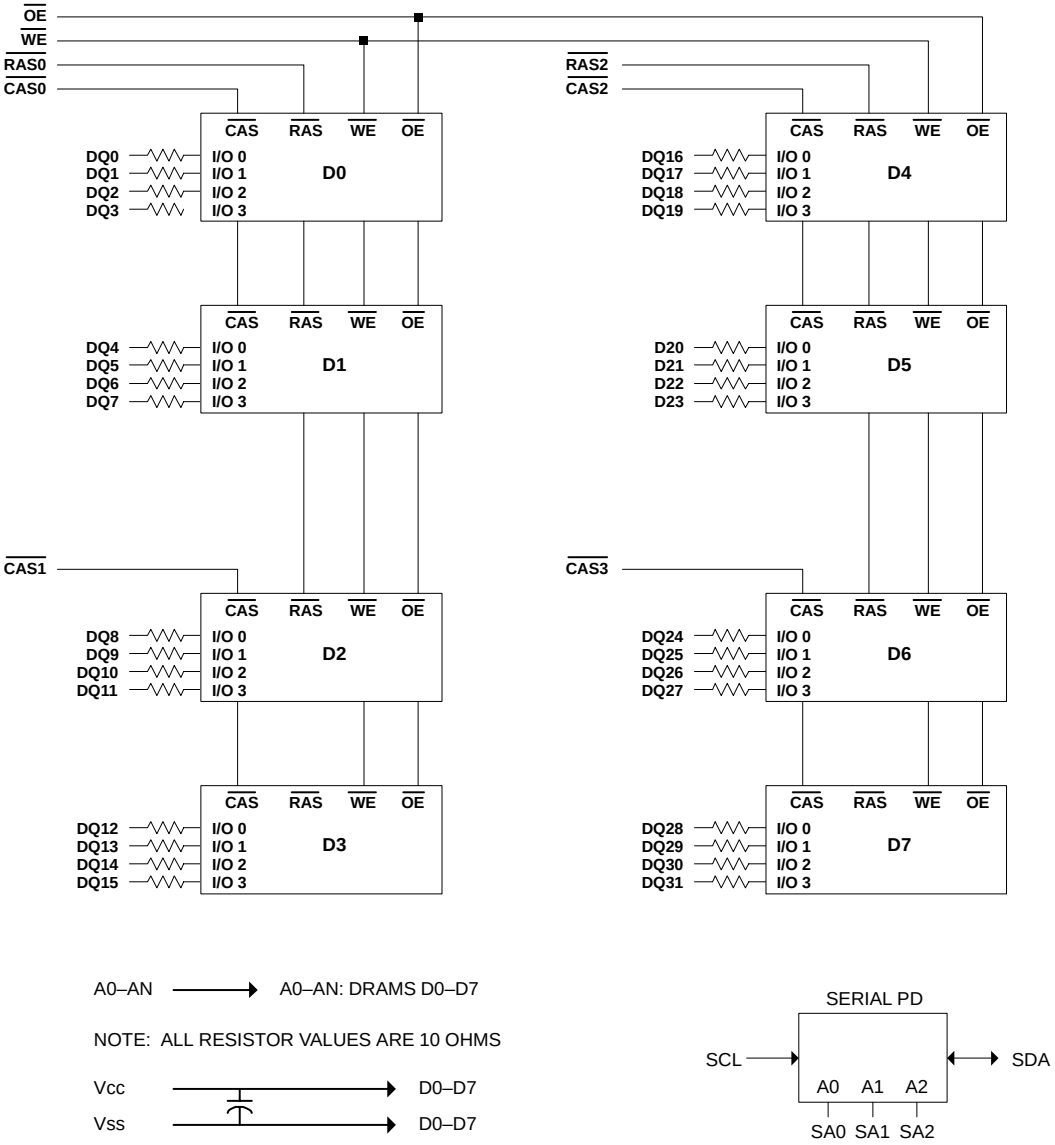


Figure 4.4.8–AA
100 Pin X32 DRAM DIMM, 1 Bank with X4 DRAMs

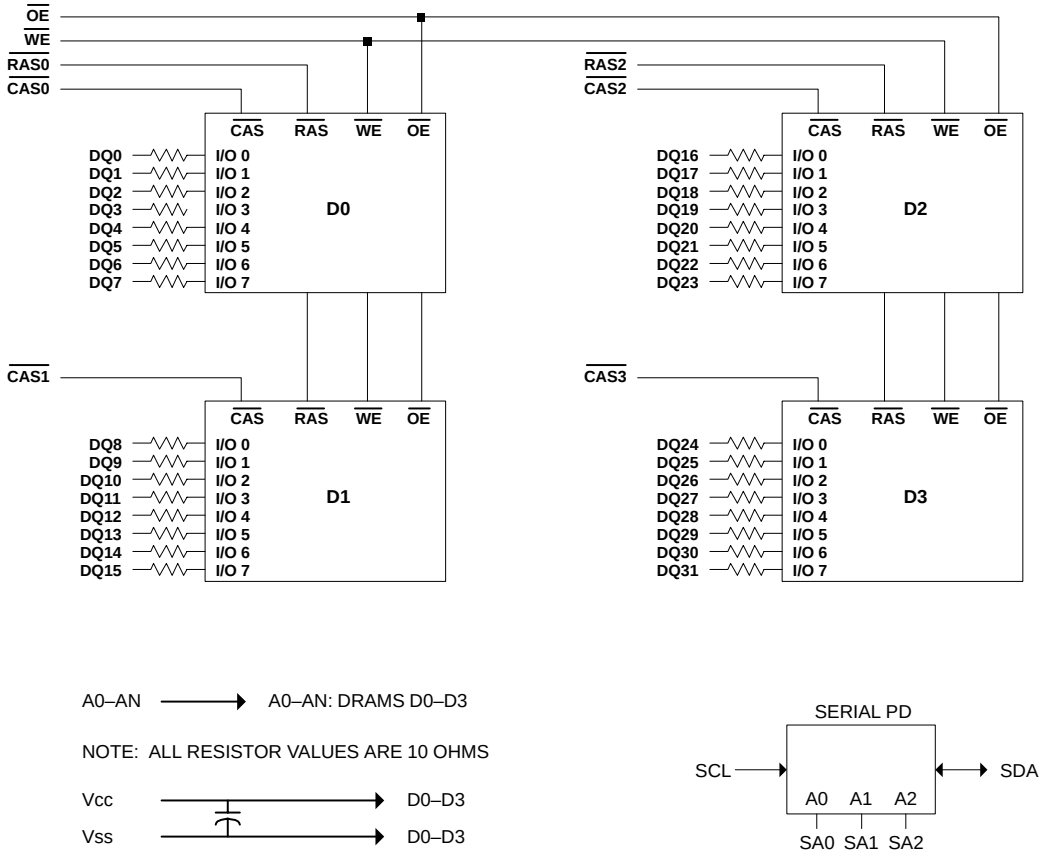


Figure 4.4.8–AB
100 Pin X32 DRAM DIMM, 1 Bank with X8 DRAMs

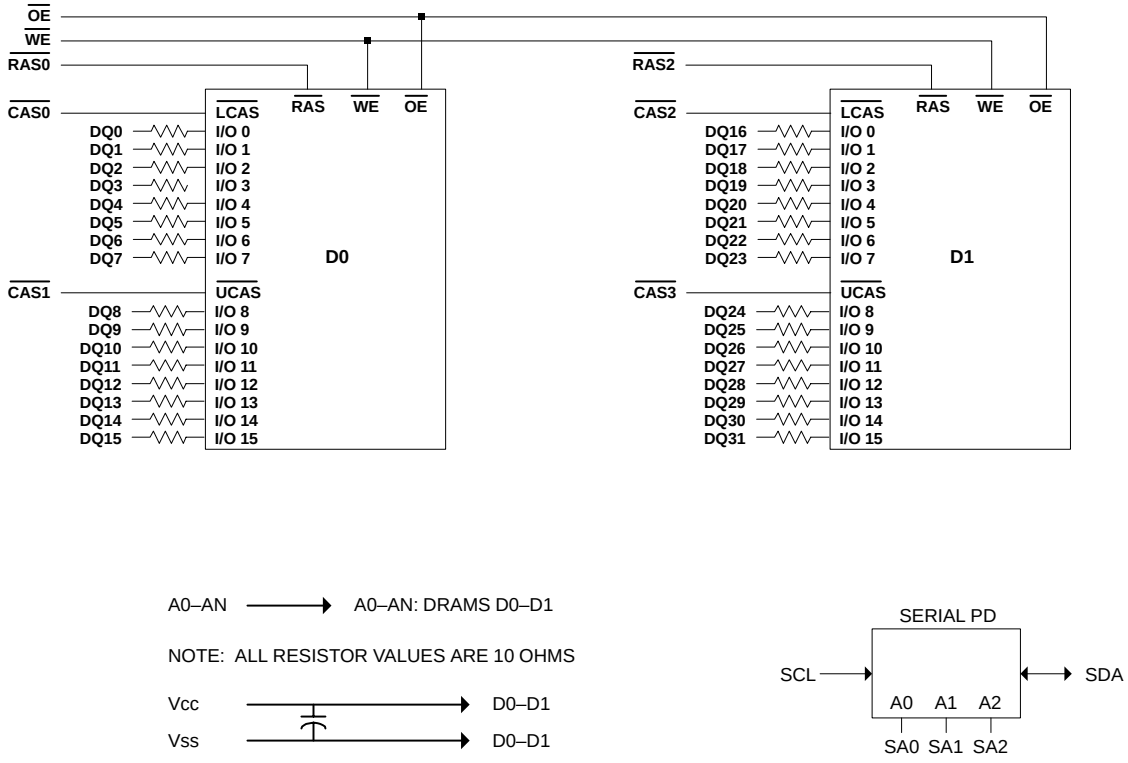


Figure 4.4.8–AC
100 Pin X32 DRAM DIMM, 1 Bank with X16 DRAMs

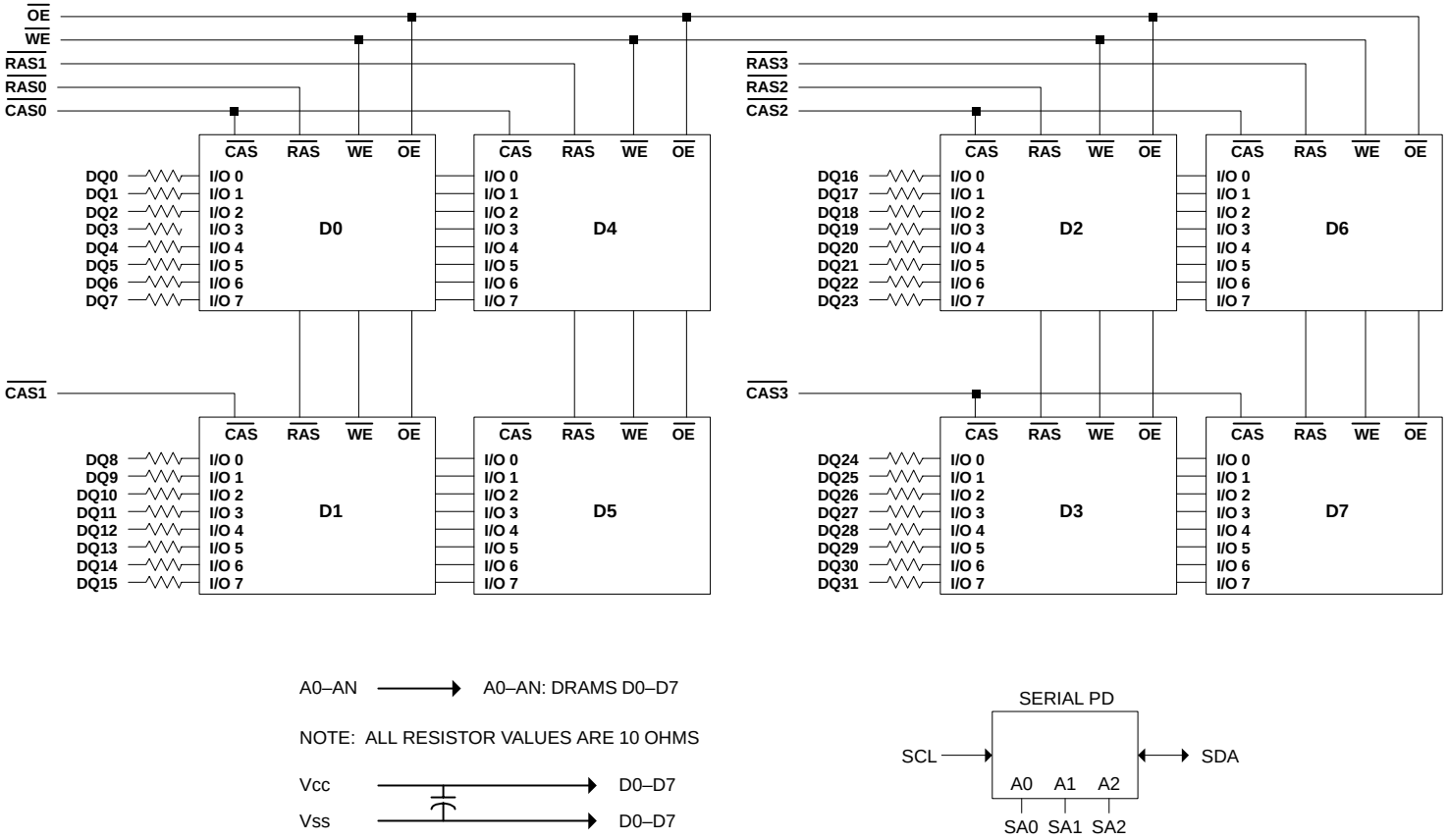


Figure 4.4.8–AD
100 Pin X32 DRAM DIMM, 2 Bank with X8 DRAMs

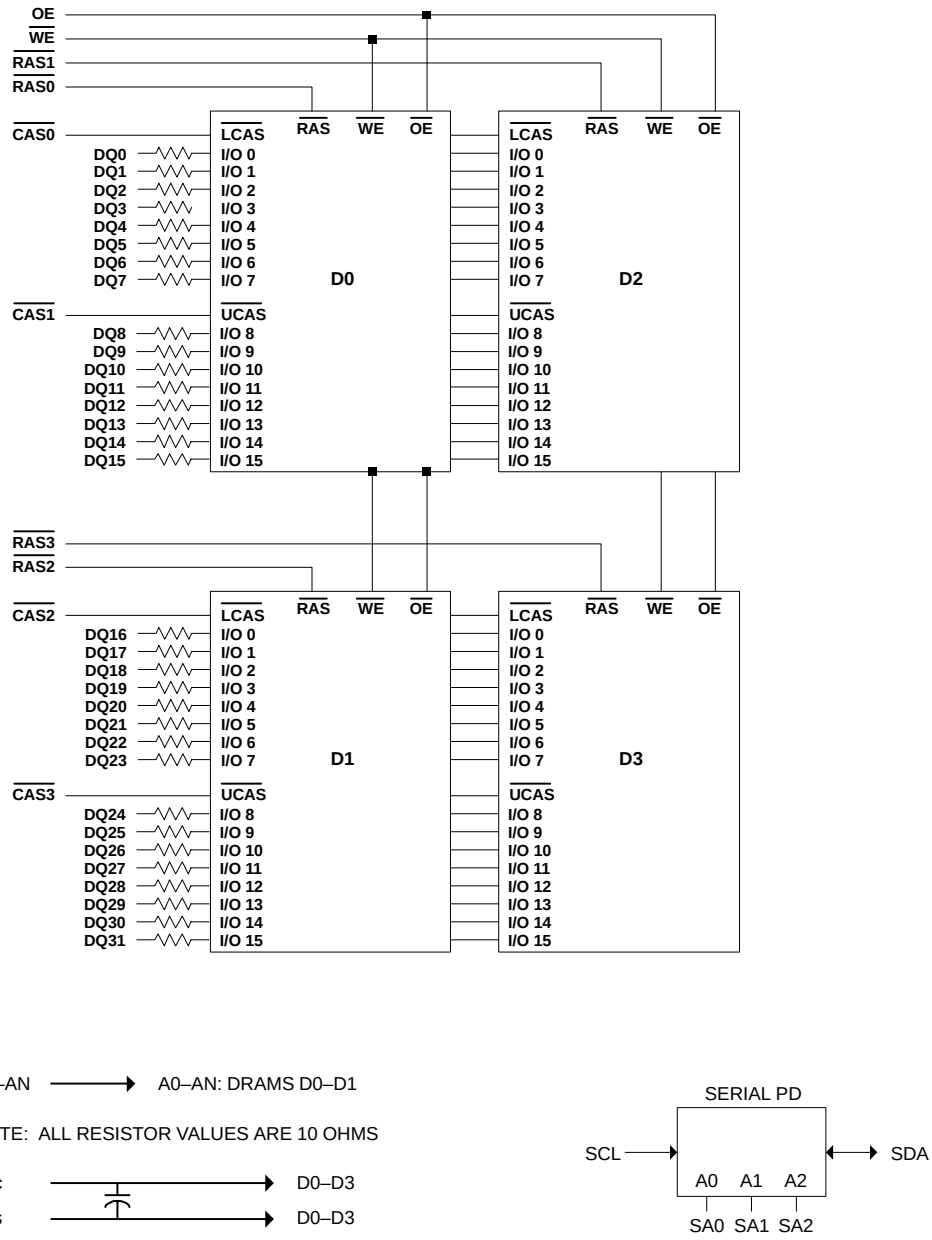


Figure 4.4.8–AE
100 Pin X32 DRAM DIMM, 2 Bank with X16 DRAMs